


# B450 AORUS M

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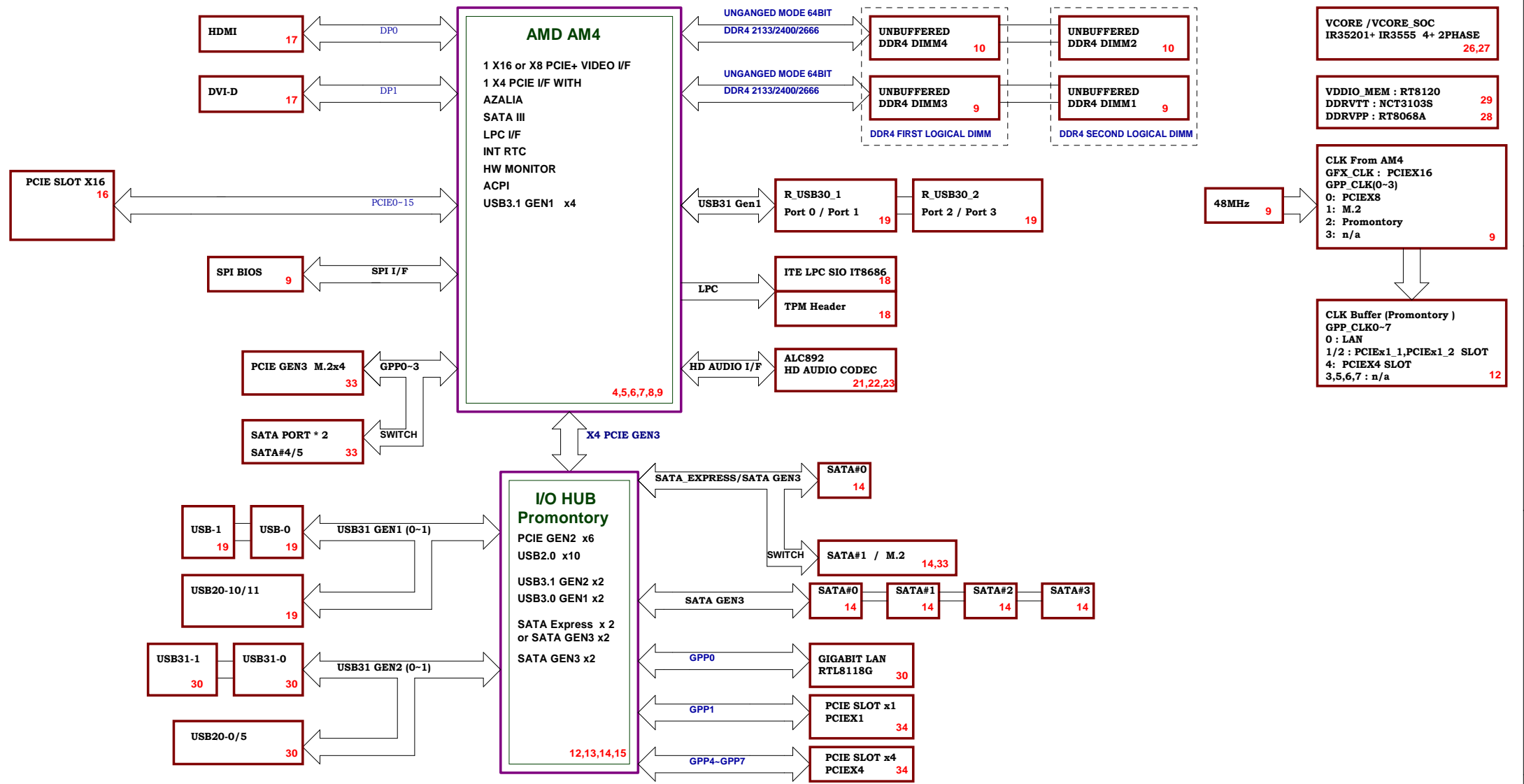
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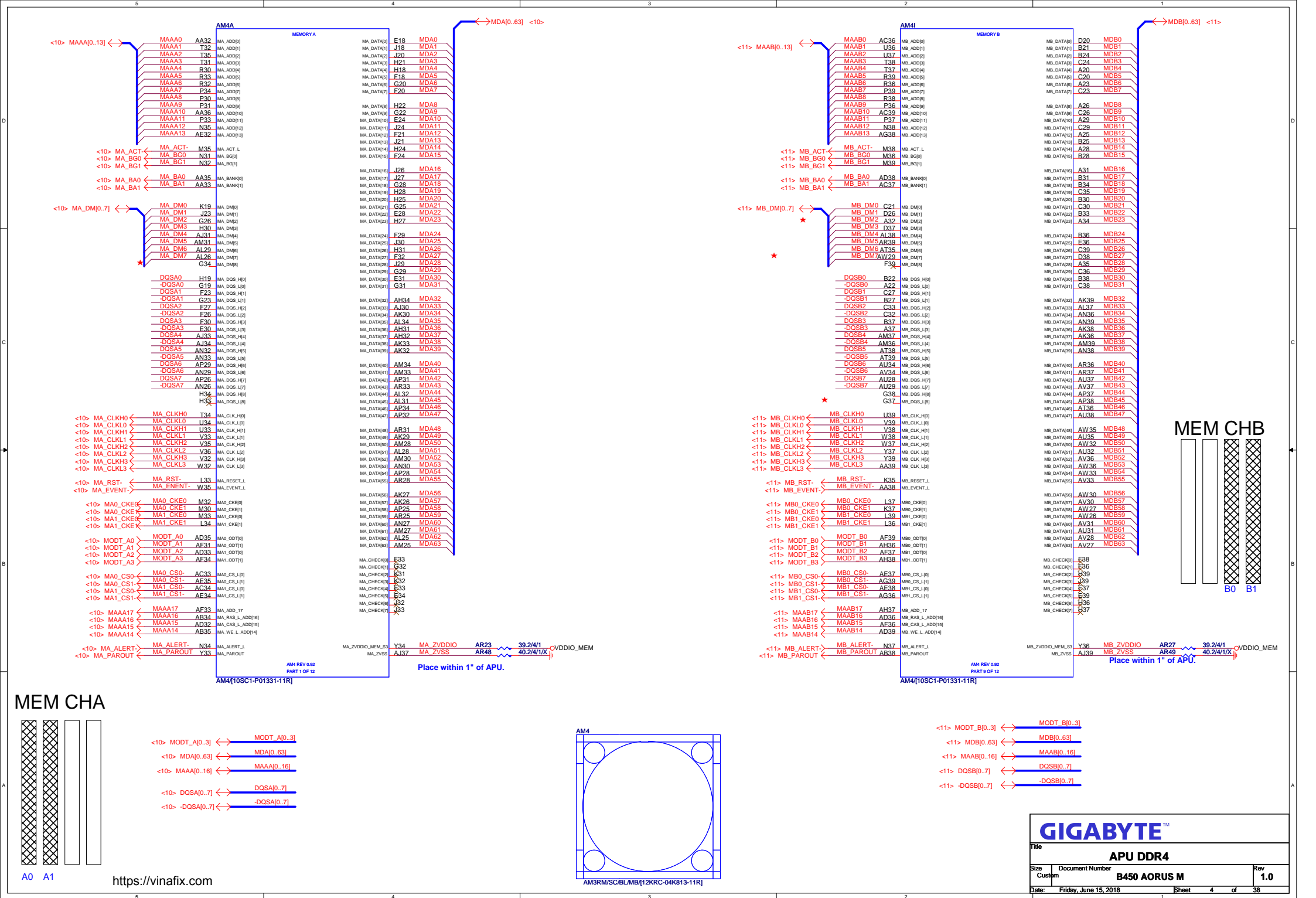
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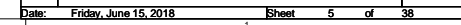
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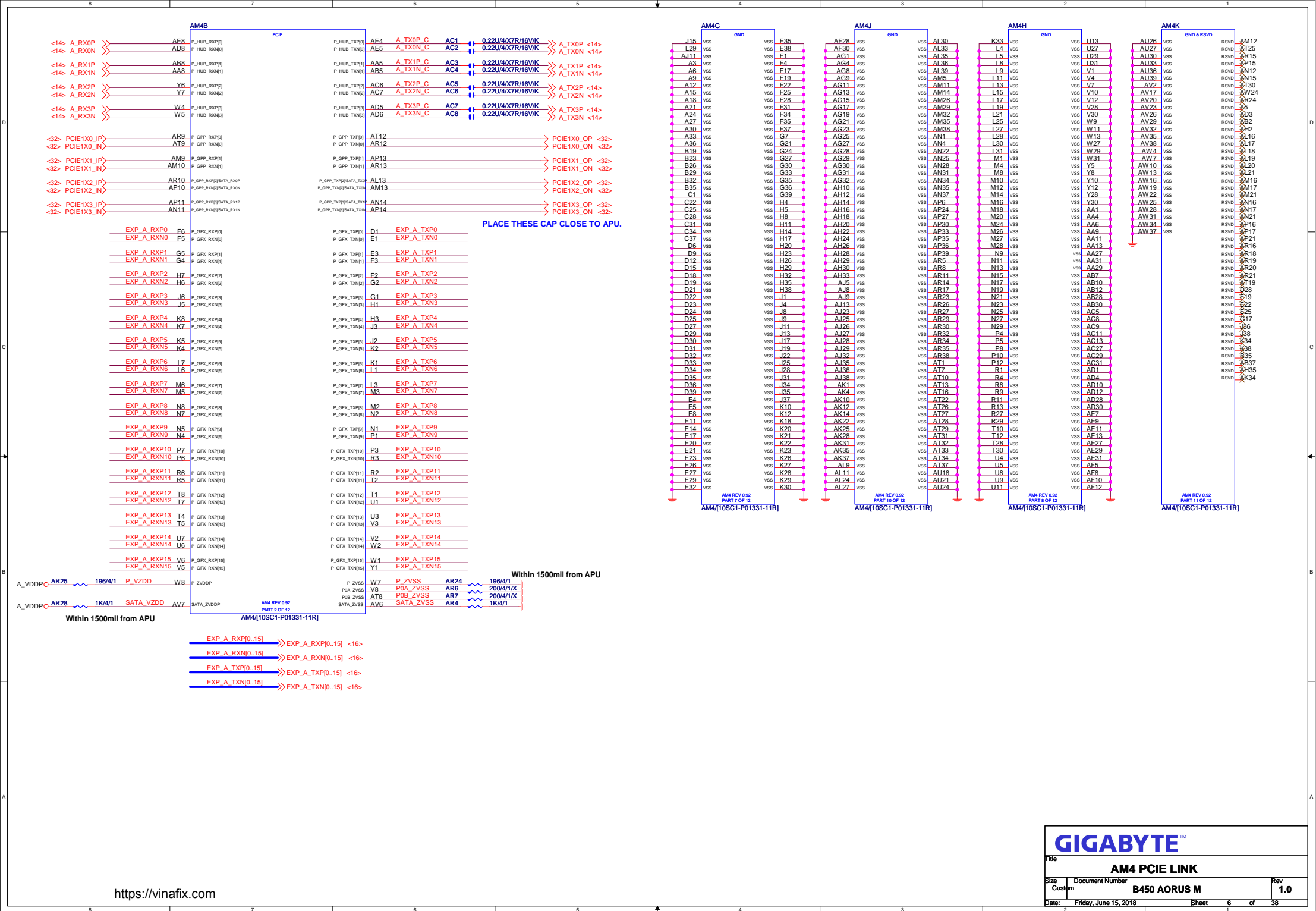
			
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Size	Document Number	<b>B450 AORUS M</b>	Rev
Custom			<b>1.0</b>
Date: <b>Friday, June 15, 2018</b>		Sheet <b>1</b> of <b>38</b>	

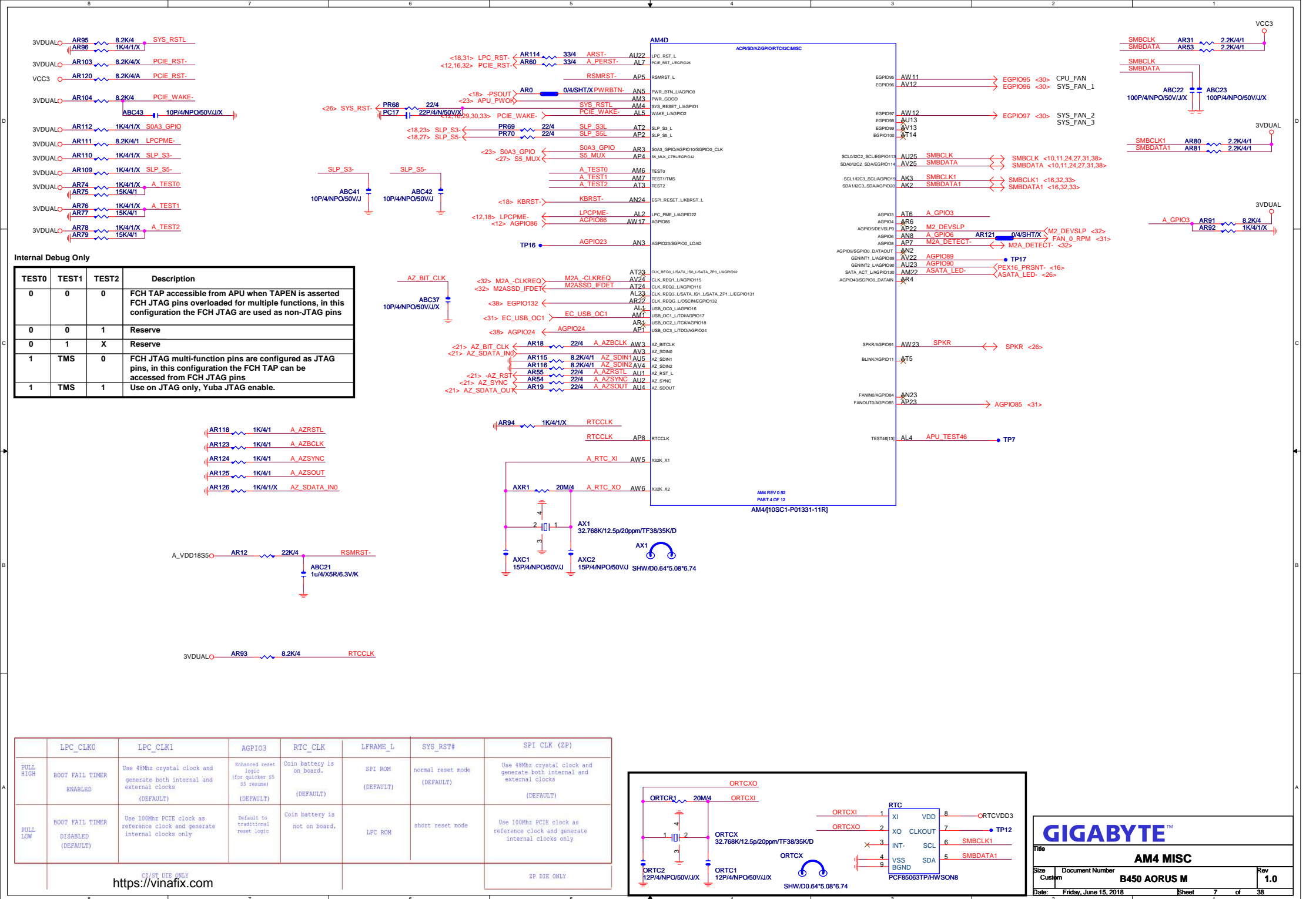
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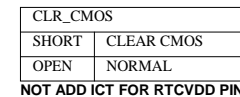
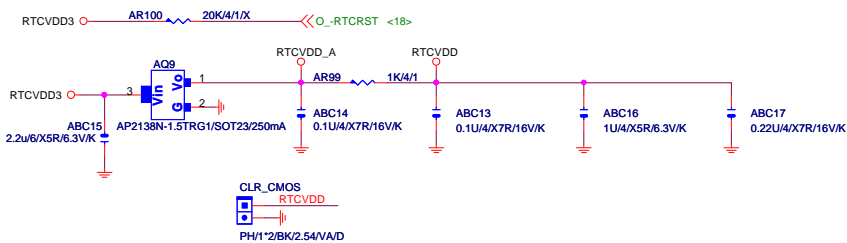




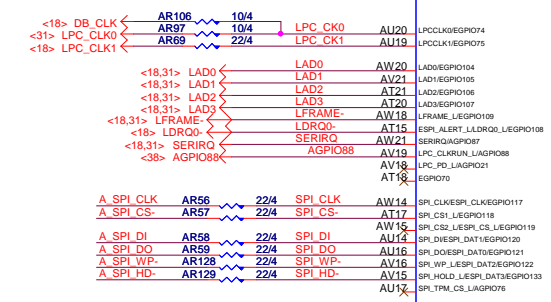
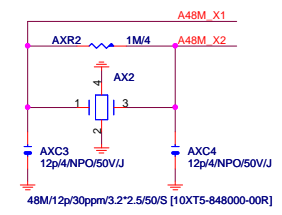
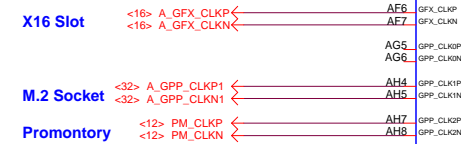
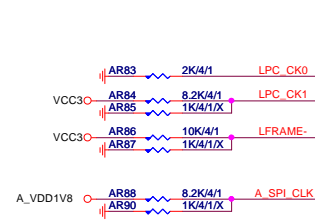






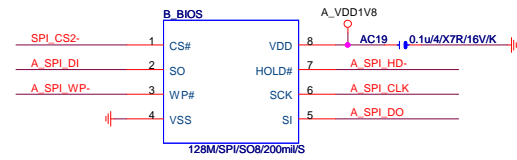
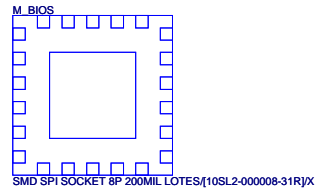
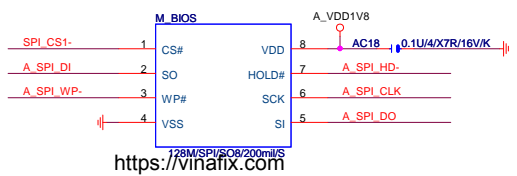
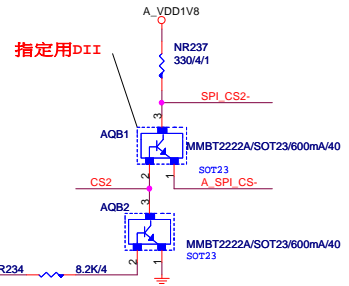
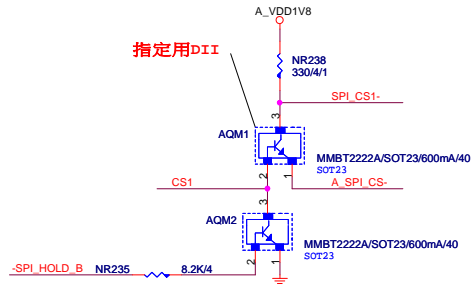
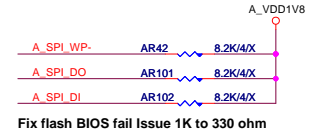






★1.8V SPI ROM USE

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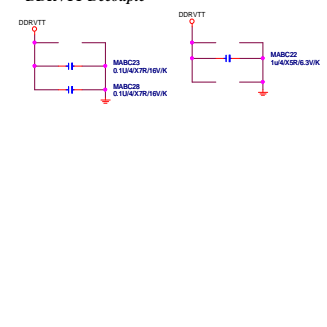
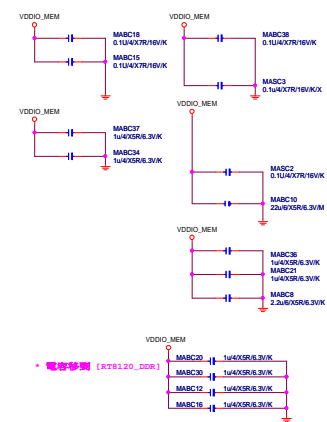
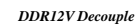
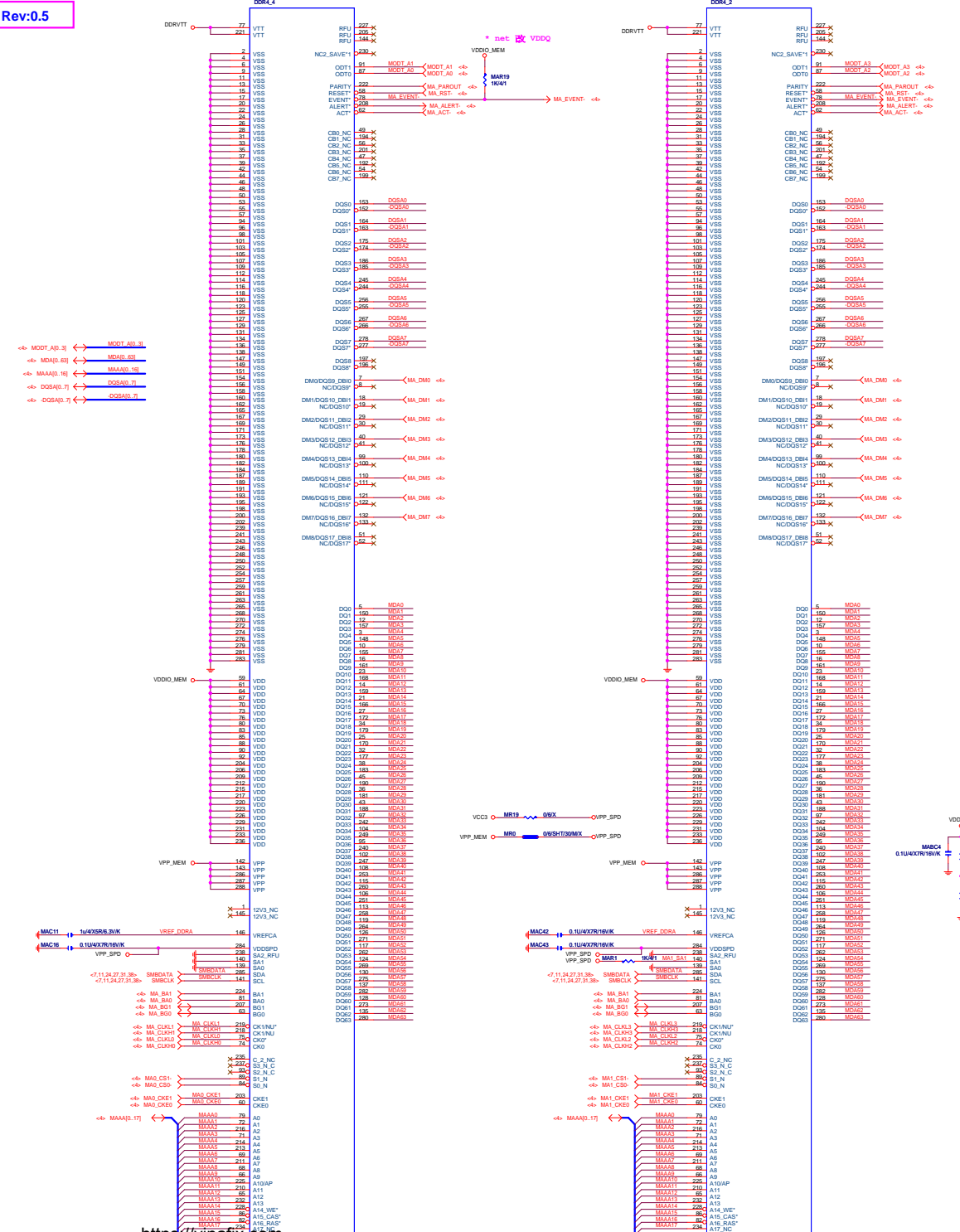


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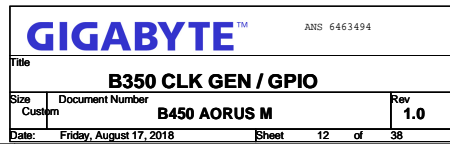
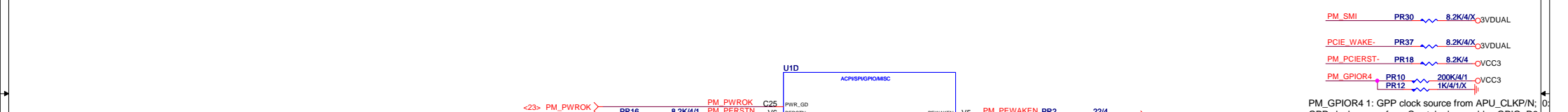
Title: **DDR4 CHANNEL A**

Size: Custom Document Number: **B450 AORUS M** Rev: **1.0**

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USB port power control 13:0 (VCC3). Output.

<29> -USBOC\_R1  
<19> -USBOC\_F1

PR62 12.1K/4/1 P\_UREXT AF10 UREXT

<19> P\_SS\_RX0P P\_SS\_RX0P AB15 USB\_SS\_RXP0  
<19> P\_SS\_RX0N P\_SS\_RX0N AC15 USB\_SS\_RXN0

<19> P\_SS\_RX1P P\_SS\_RX1P AC16 USB\_SS\_RXP1  
<19> P\_SS\_RX1N P\_SS\_RX1N AB16 USB\_SS\_RXN1

AB18 USB\_SS\_RXP2  
AC18 USB\_SS\_RXN2

AC19 USB\_SS\_RXP3  
AB19 USB\_SS\_RXN3

AC21 USB\_SS\_RXP4  
AB21 USB\_SS\_RXN4

AF24 USB\_SS\_RXP5  
AE24 USB\_SS\_RXN5

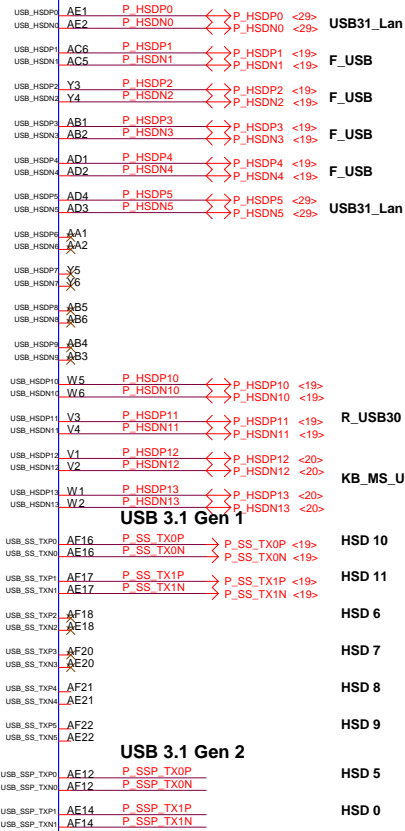
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P\_SSP\_RX0N AA11 USB\_SS\_RXN0  
P\_SSP\_RX1P AC13 USB\_SS\_RXP1  
P\_SSP\_RX1N AB13 USB\_SS\_RXN1

PROMOTORY REV 0.3

218-0891011/S

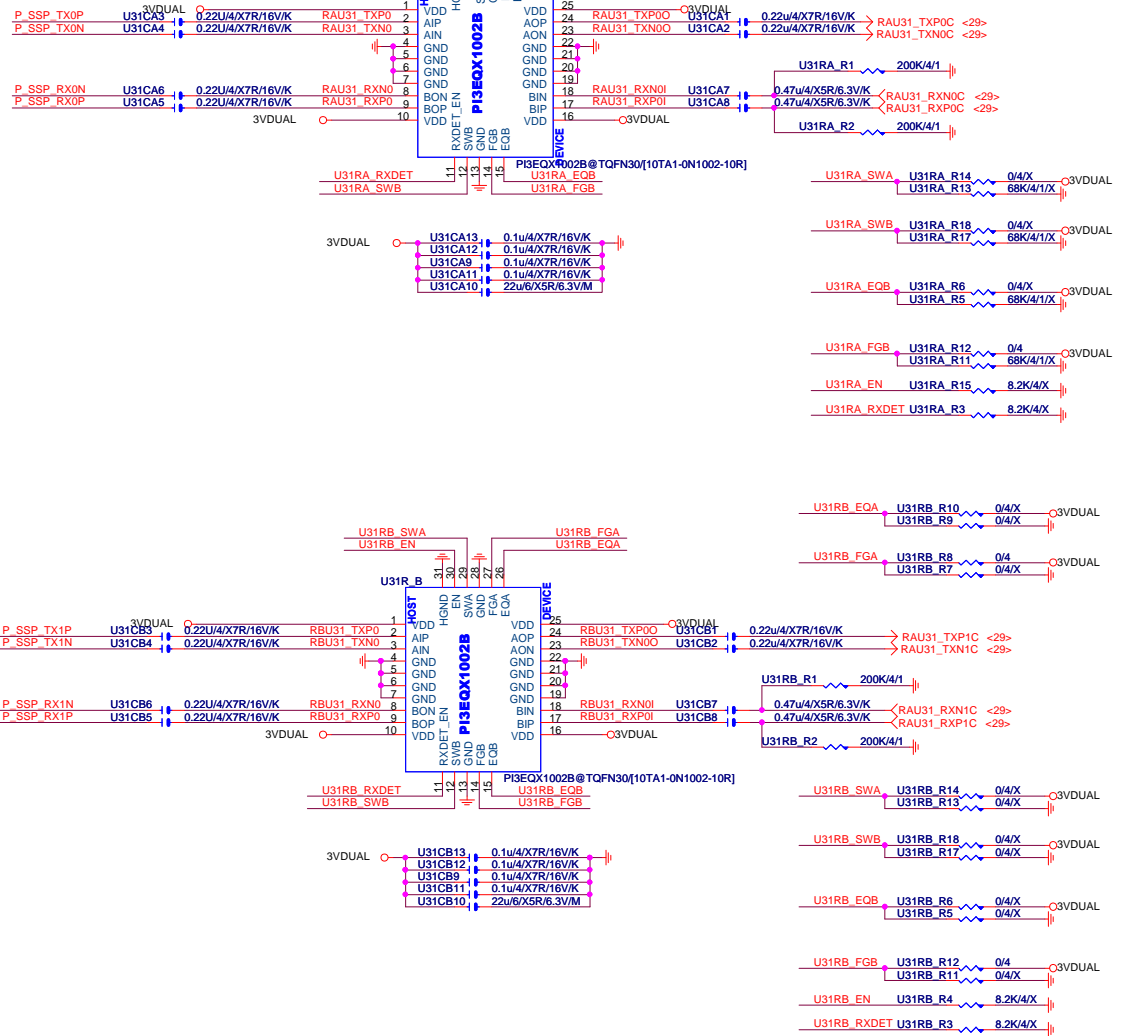
BUS Model	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

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### USB 3.1 Gen 1

### USB 3.1 Gen 2

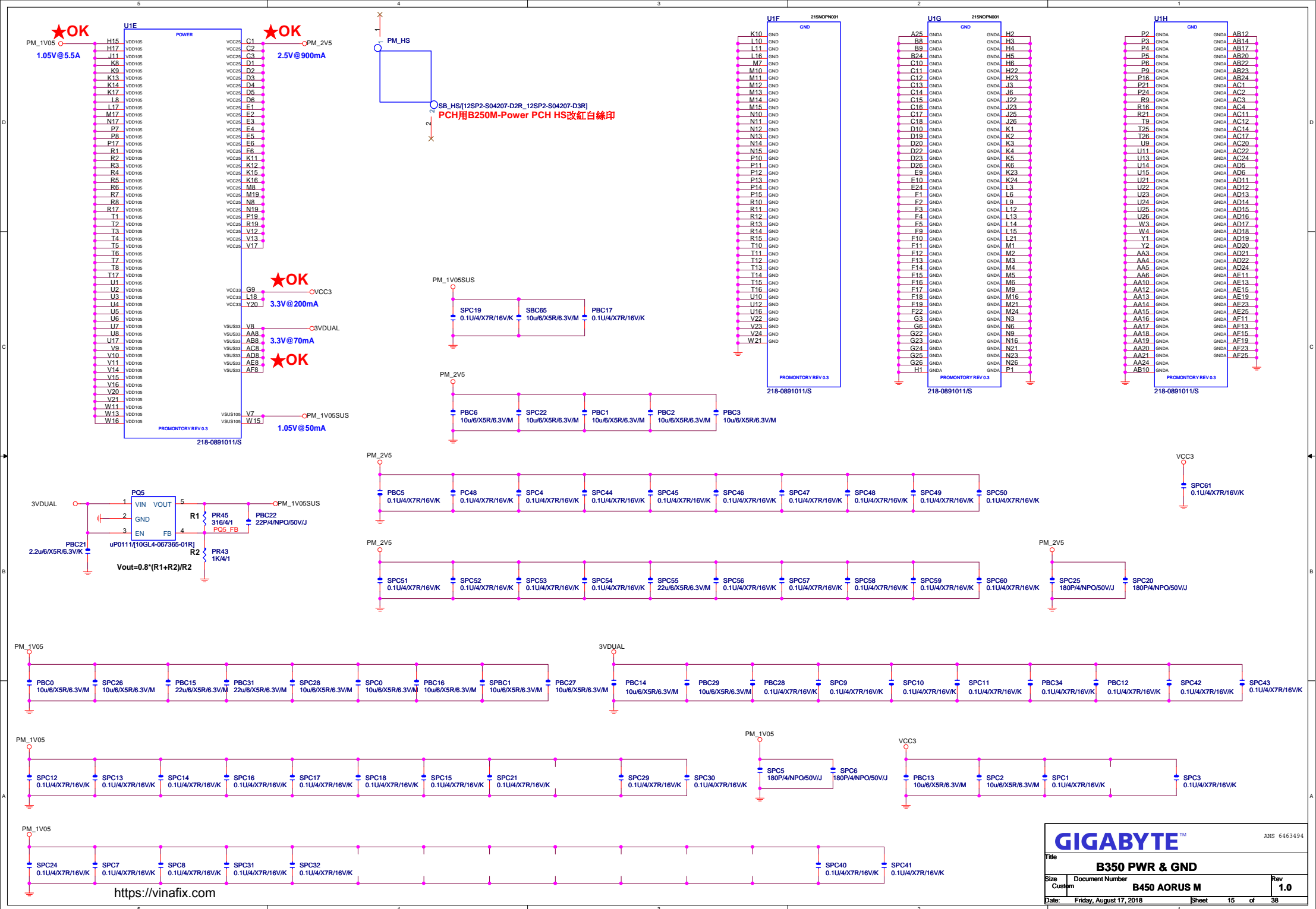


BUS Model	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

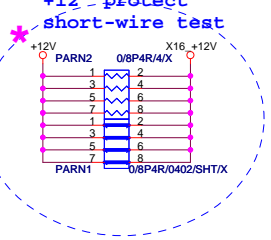
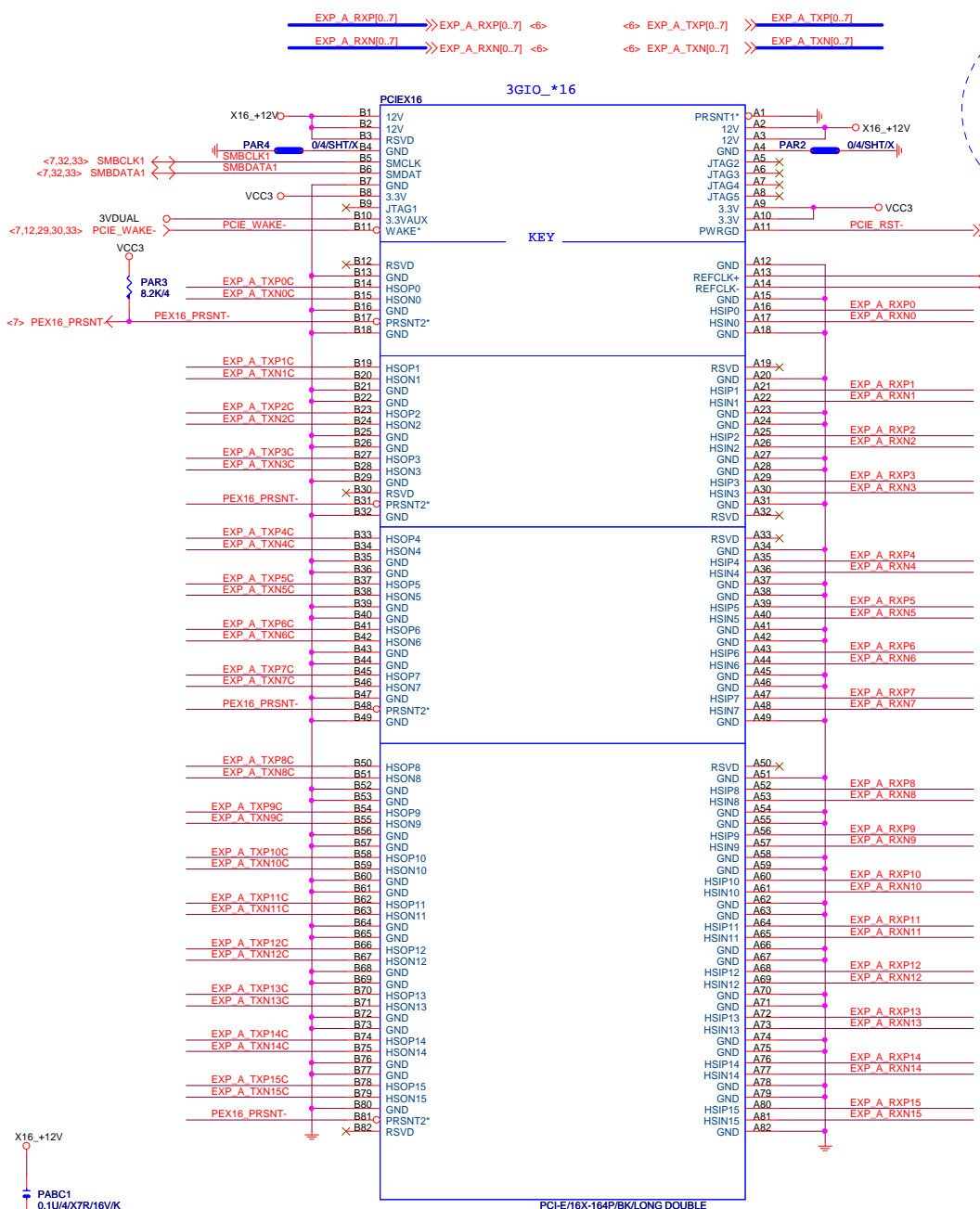
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Date: Friday, August 17, 2018  
Document Number  
**B450 AORUS M**  
Rev  
**1.0**

ASIS 6463494  
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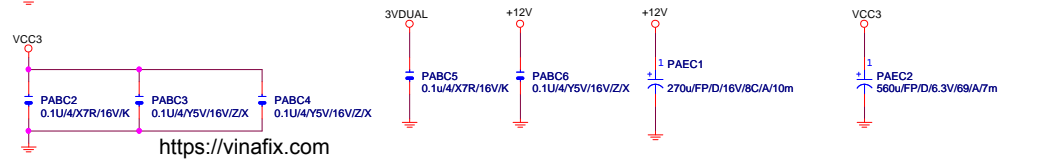






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EXP A TXN0	PAC5	0.22u/4X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4X5R6.3V/K	EXP A TXP10C
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EXP A TXP13	PAC30	0.22u/4X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4X5R6.3V/K	EXP A TXN15C

EXP A RXP[0..15]	>>>EXP_A_RXP[0..15] <->
EXP A RXN[0..15]	>>>EXP_A_RXN[0..15] <->
EXP A TXP[0..15]	>>>EXP_A_TXP[0..15] <->
EXP A TXN[0..15]	>>>EXP_A_TXN[0..15] <->



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Size

Custom

Date:

Friday, June 15, 2018

Title

PCIEx16

Document Number

B450 AORUS M

Rev

1.0

Sheet

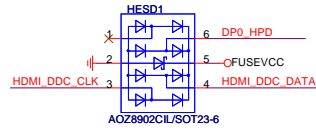
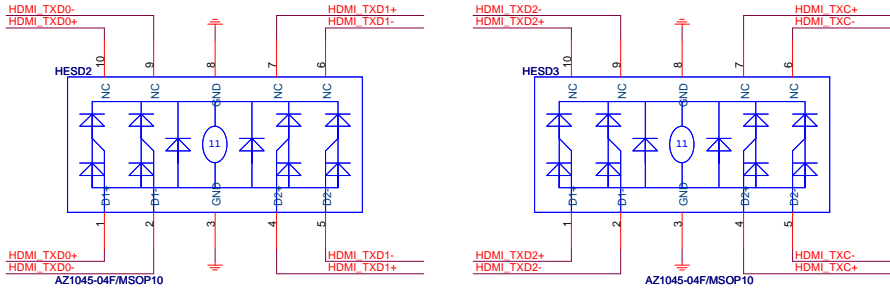
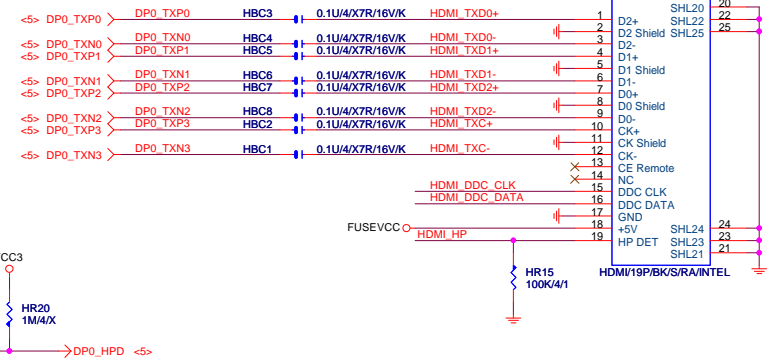
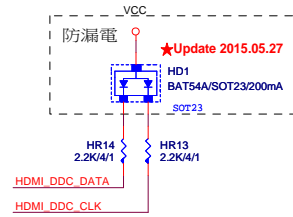
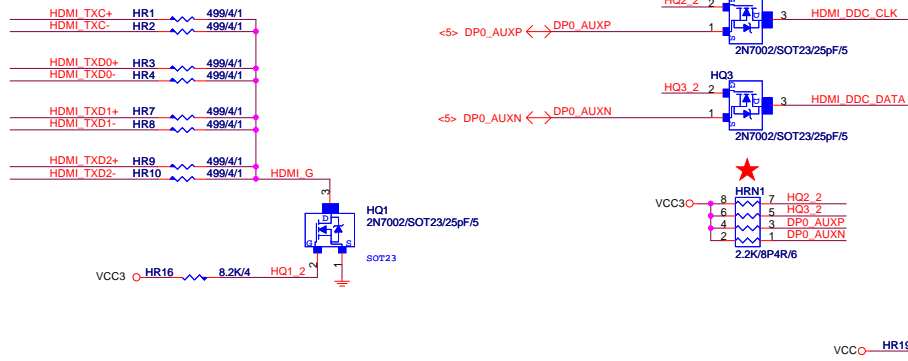
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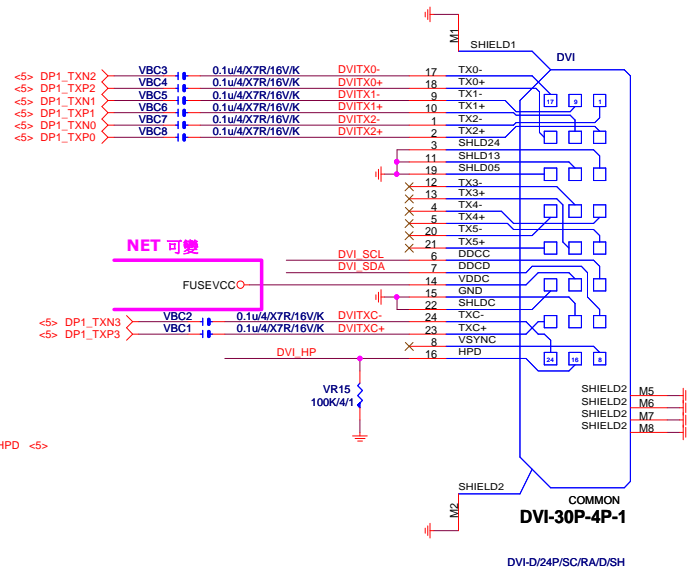
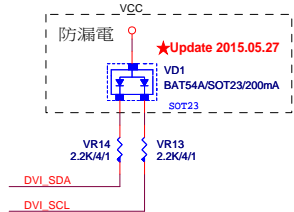
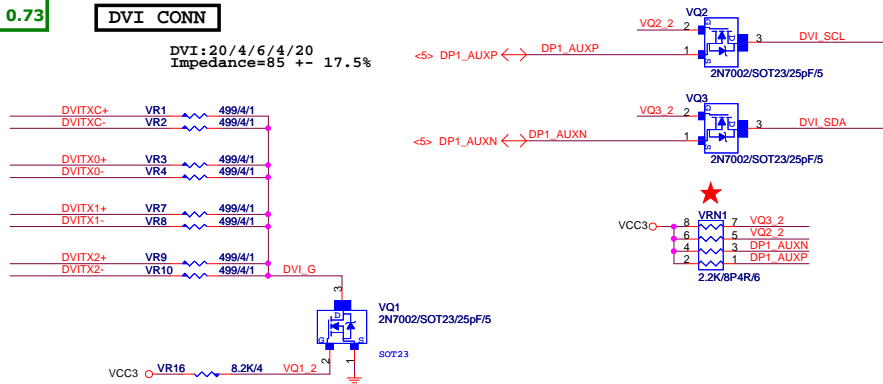




Rev: 0.73

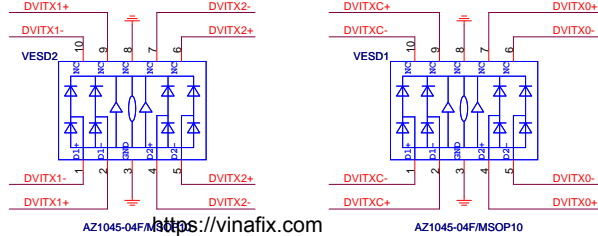
DVI CONN

DVI: 20/4/6/4/20  
Impedance=85 +- 17.5%



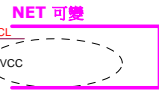
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Close to connector



NET 可變

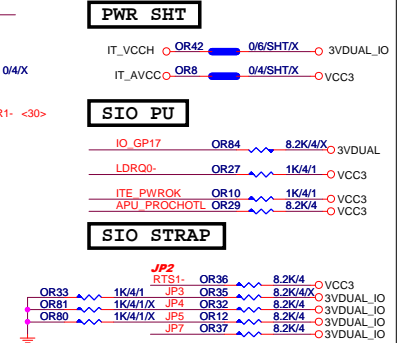
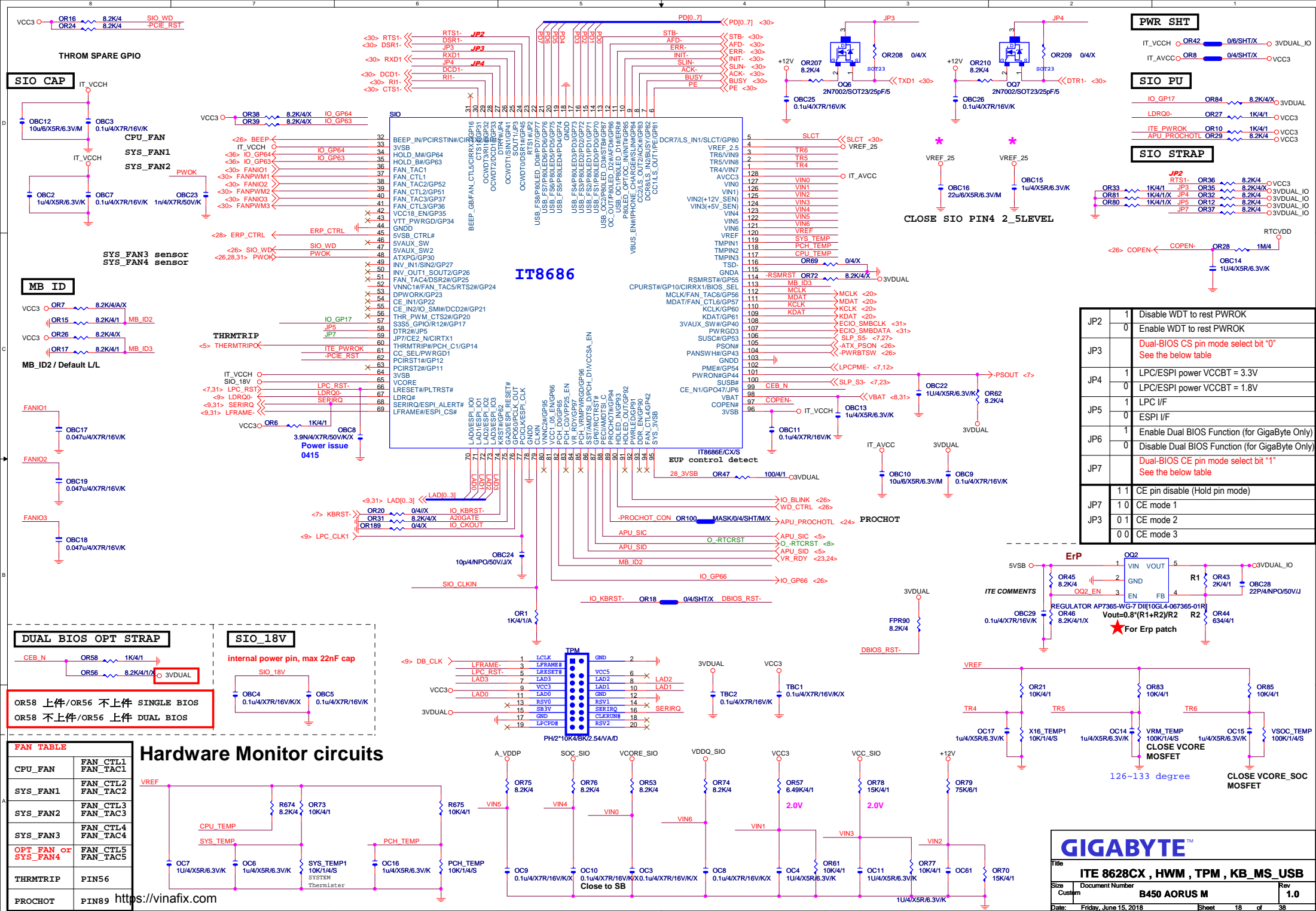
Close to connector



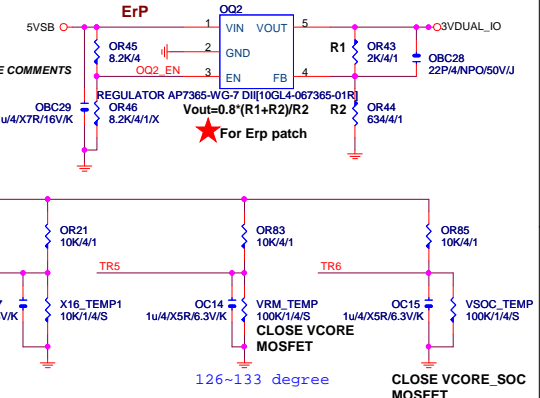
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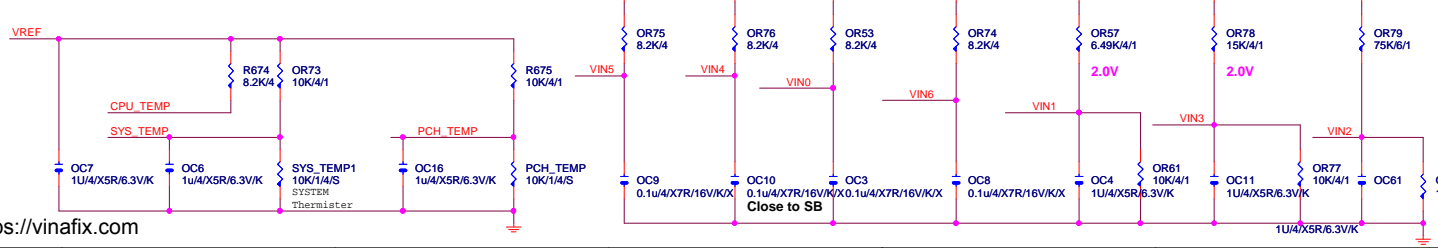
GIGABYTE™		
Title HDMI, DVI		
Size Custom	Document Number B450 AORUS M	Rev 1.0
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JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3

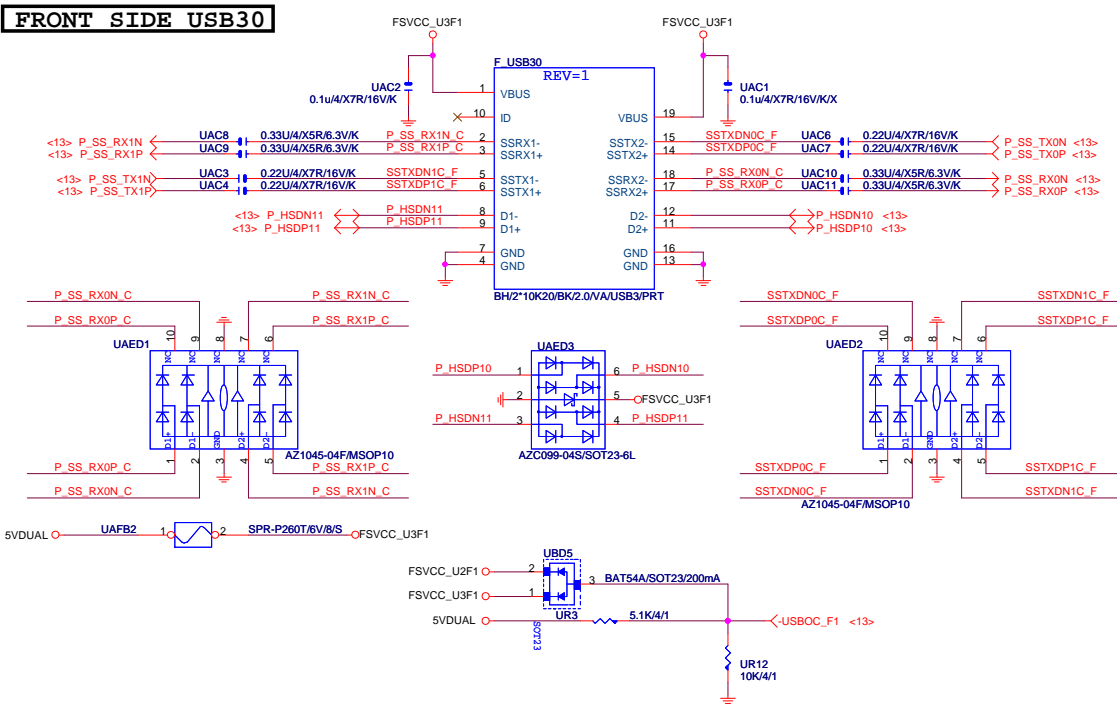


### Hardware Monitor circuits

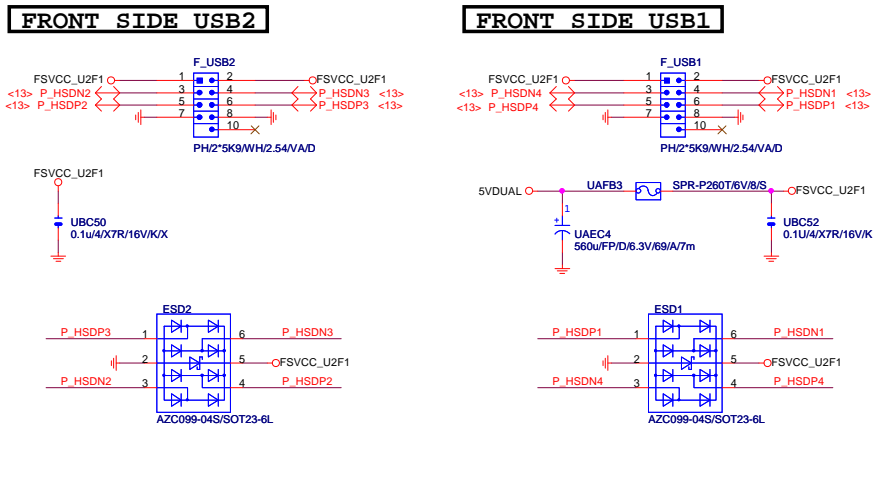


FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTrip	PIN56
PROCHOT	PIN89

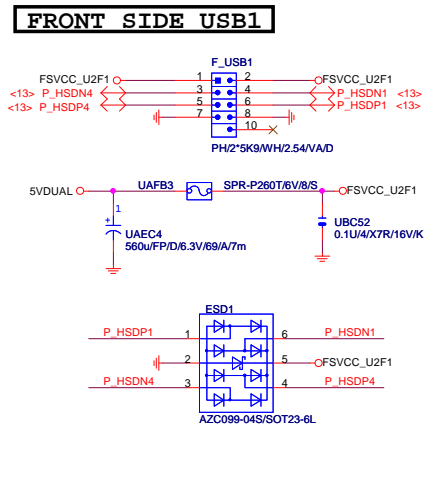
FRONT SIDE USB30



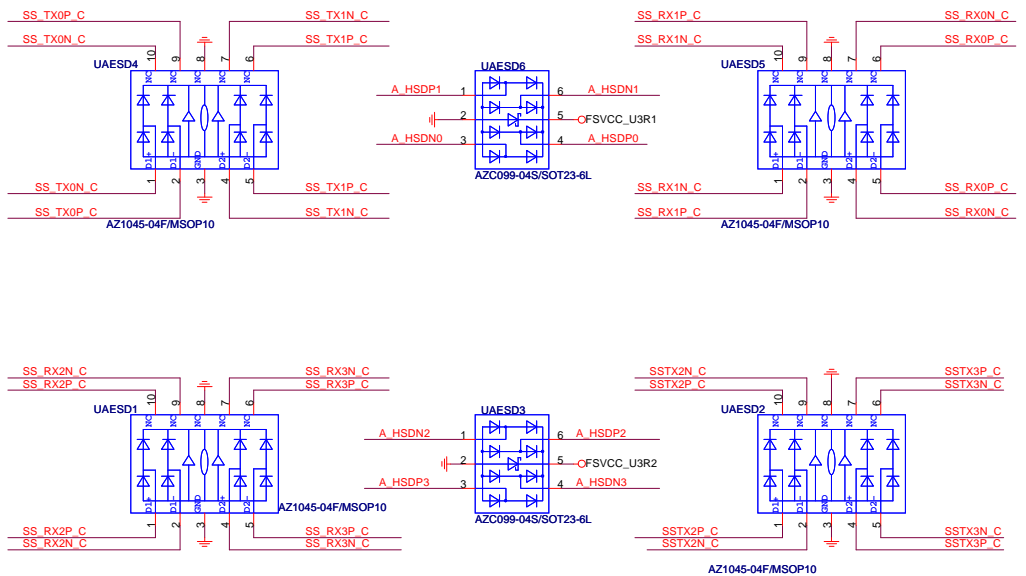
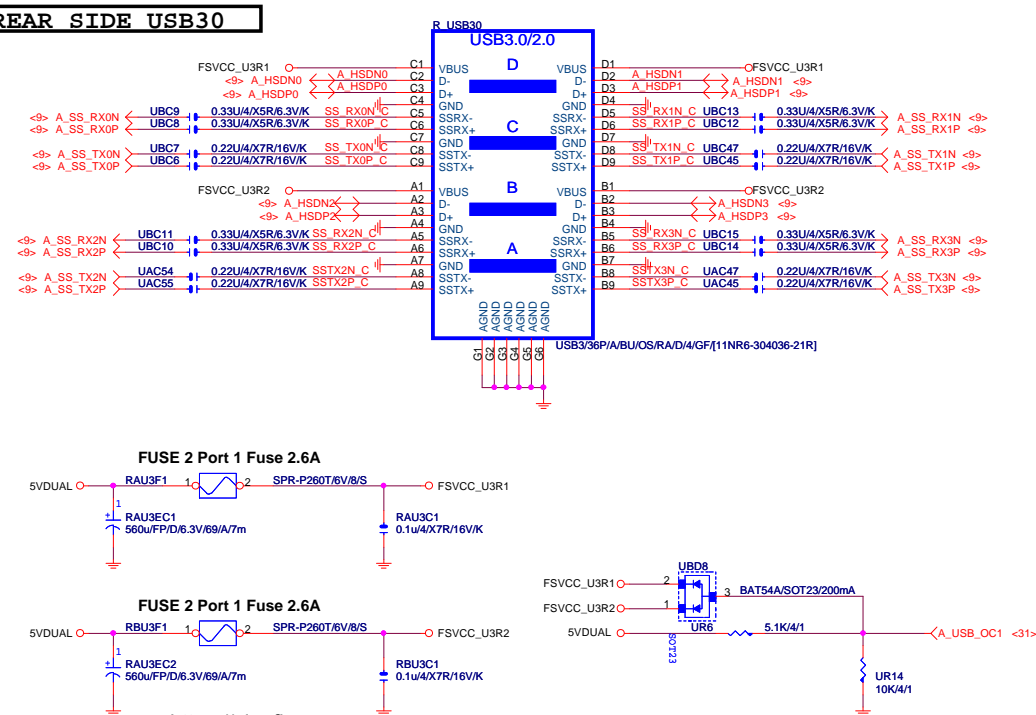
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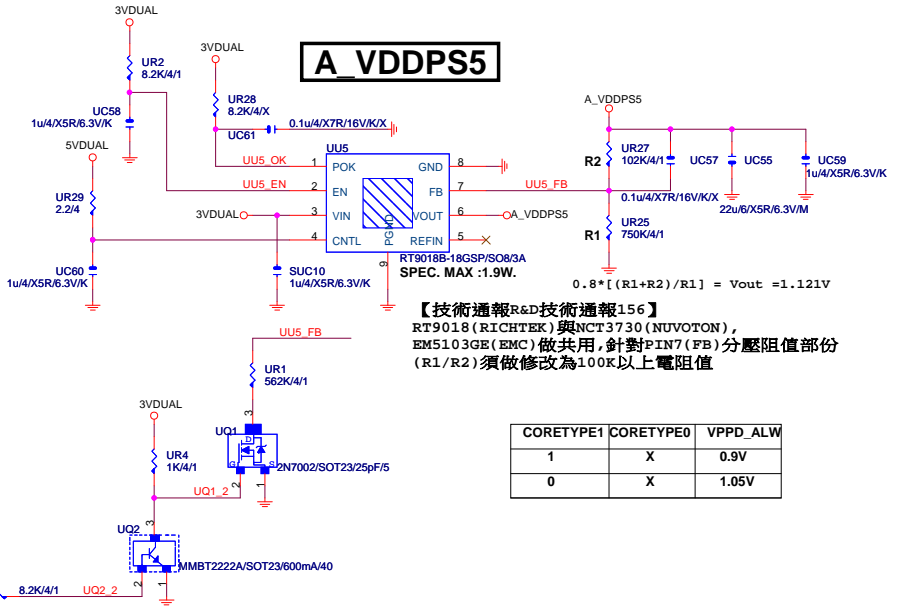
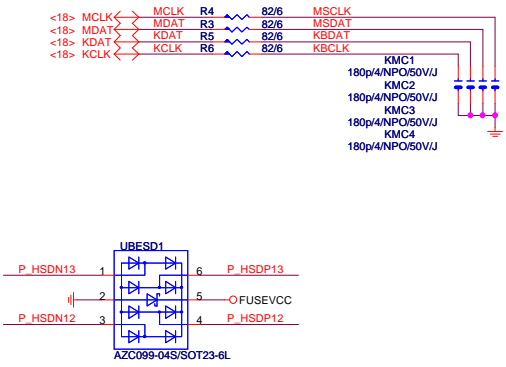
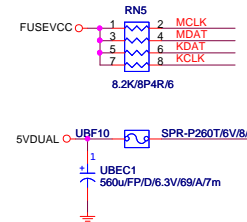
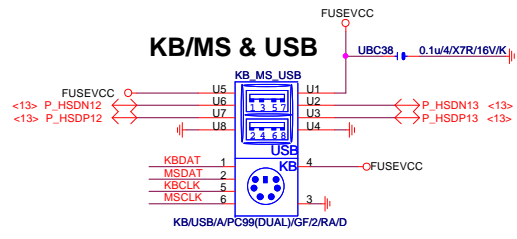


## FRONT SIDE USB1



## REAR SIDE USB30

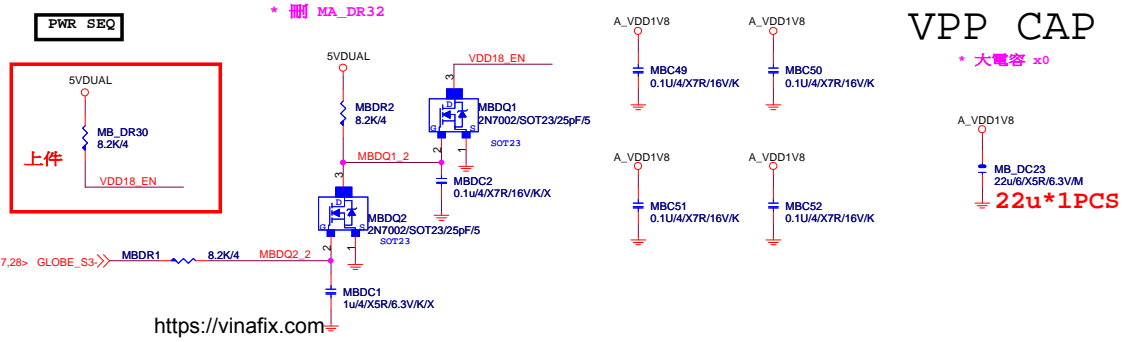
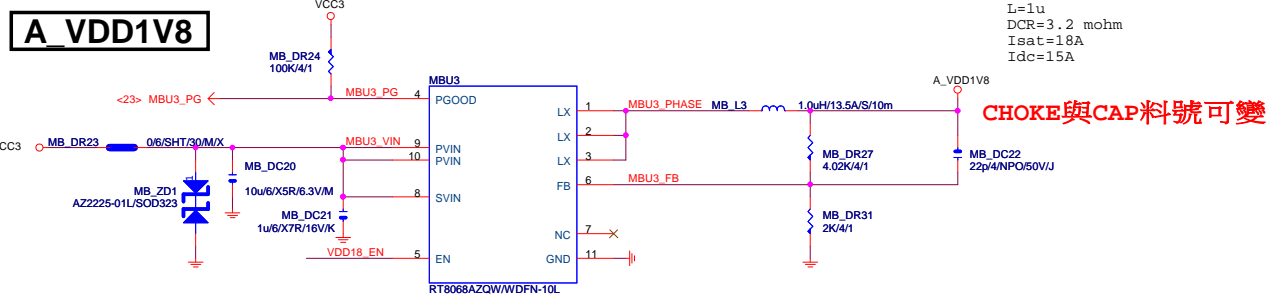




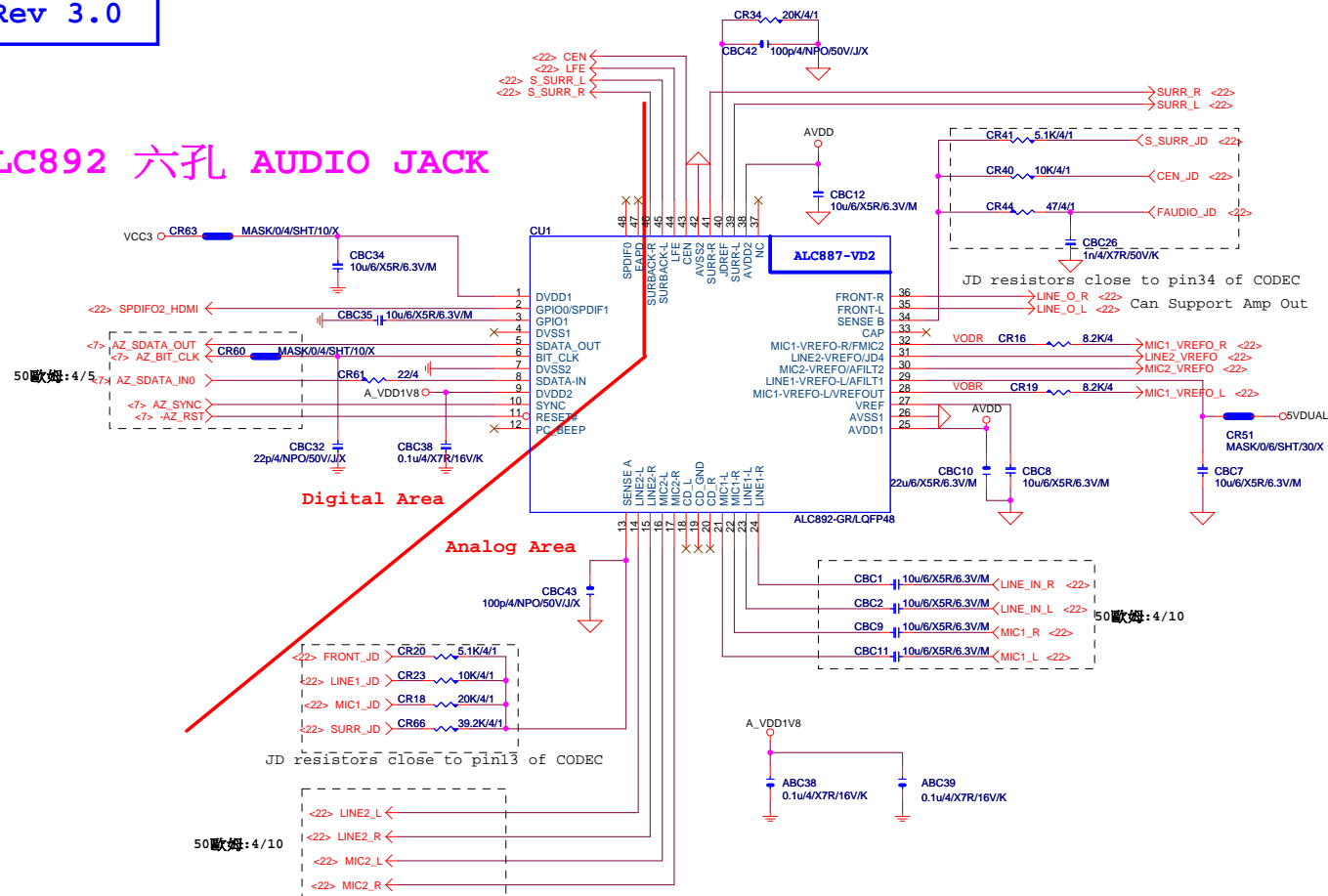
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

REV:0.4

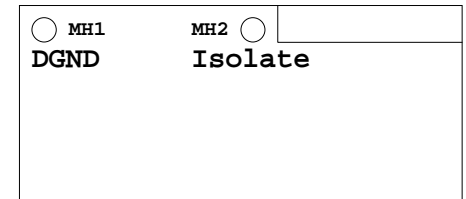
## A\_VDD1V8



## ALC892 六孔 AUDIO JACK



- LAYOUT注意: 螺絲孔下GND方式**
- MH1空間夠, 下DGND  
空間不夠, 才改為Isolate
  - MH2一律改為Isolate
  - Codec下方, 第二層必須參考GND



**LAYOUT注意: 要加  
GND切割線**

**音效區域印刷**

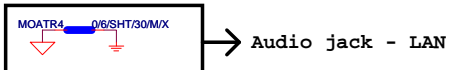
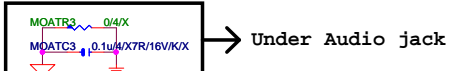


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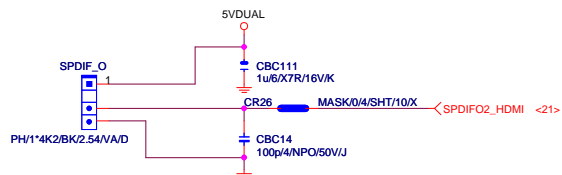
- BOM OPTION :**
- Chemicon音效電容
  - 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
  - LED Reserve (上件與否和LED顏色, 依照各Model spec)

GIGABYTE™			
Title <b>ALC887 CODEC</b>			
Size	Document Number	Rev	
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Rev 3.0

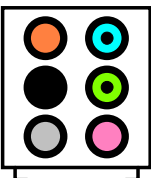


\*量産前,0ohm改short pad



For HDMI SPDIF (依SPEC保留或移除)

## AZALIA JACK



## AZALIA JACK

BLUE

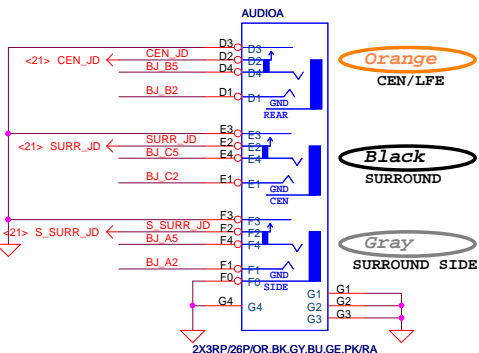
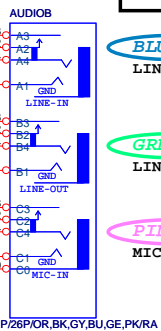
LINE-IN

GREEN

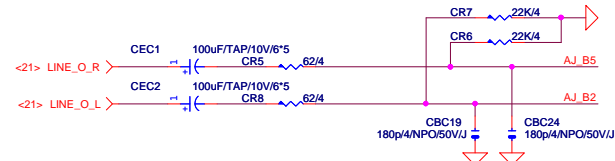
LINE-OUT

PINK

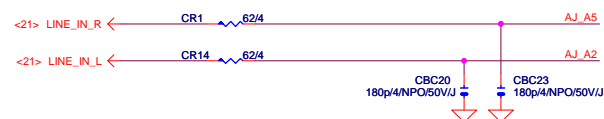
MIC-IN



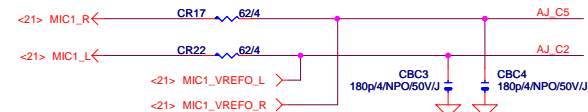
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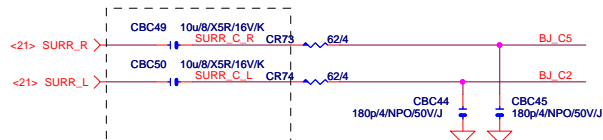
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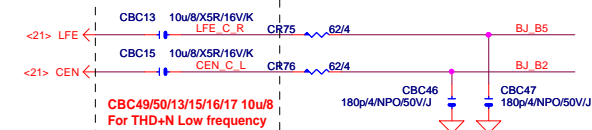
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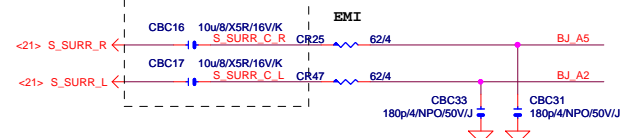
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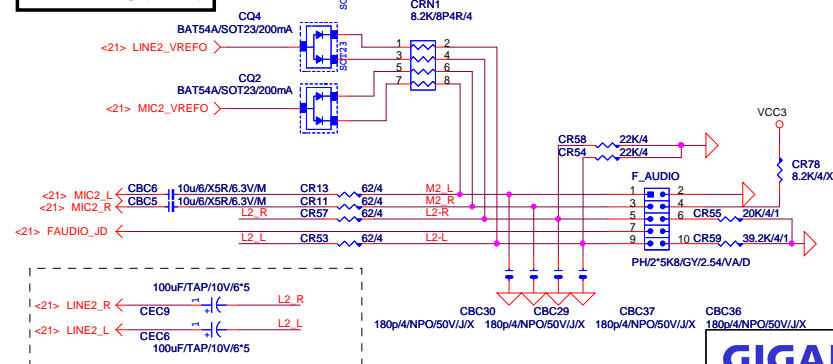
## CEN/LFE



## SURR BACK

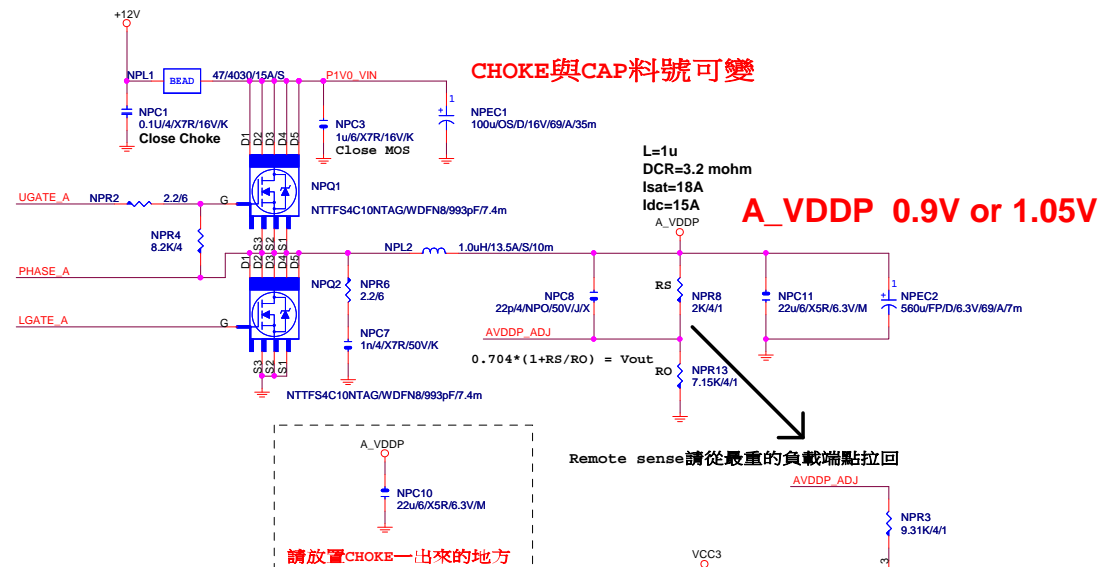
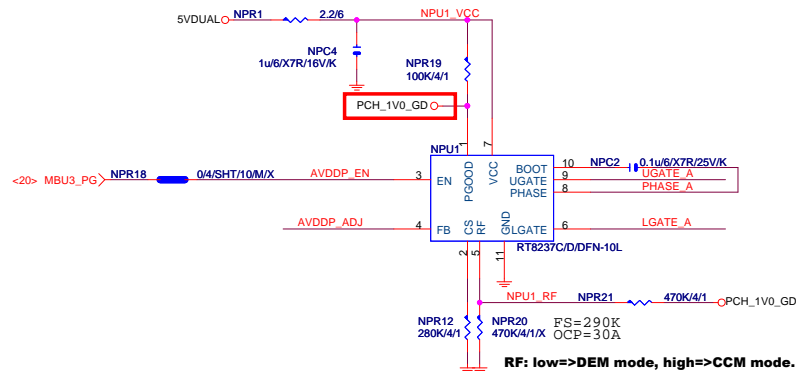


## AZALIA FRONT PANEL

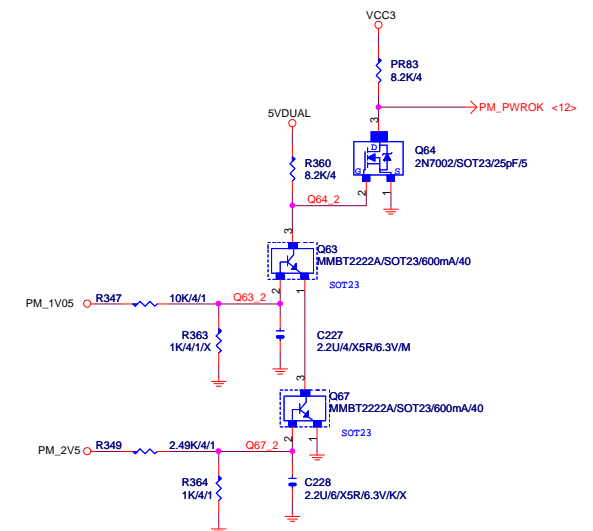
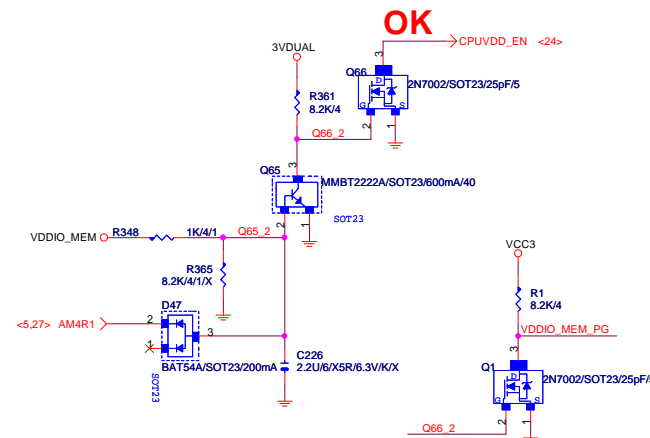
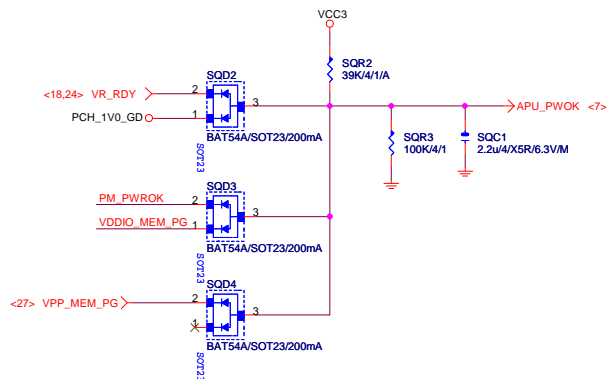
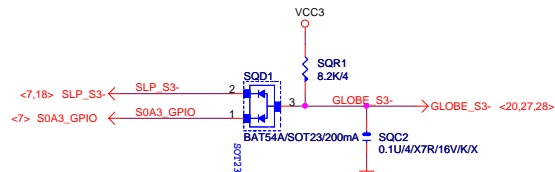


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CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V



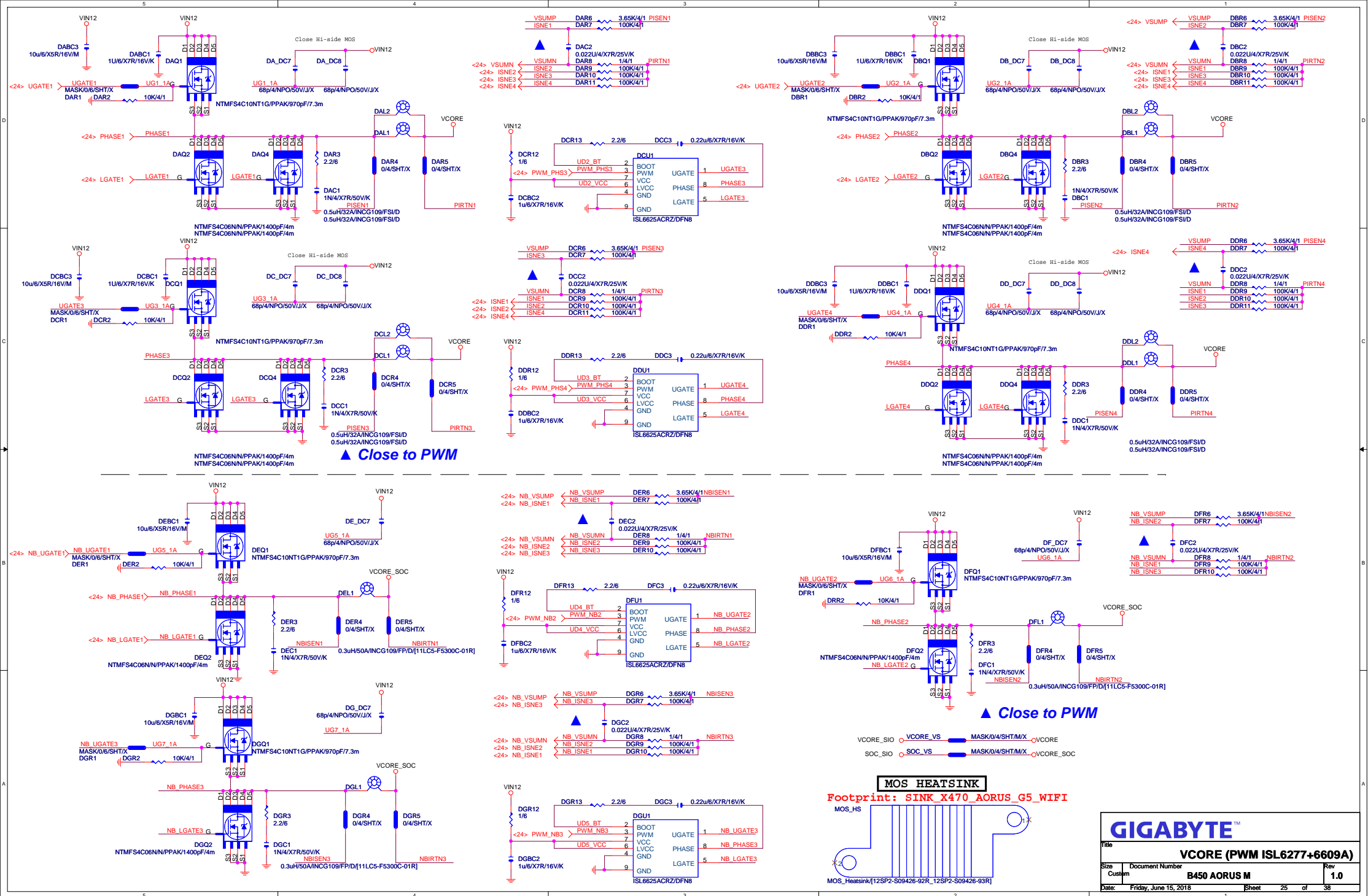
GIGABYTE™

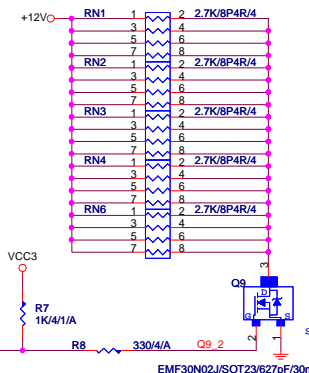
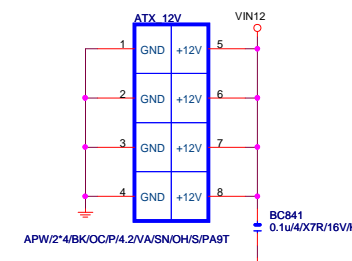
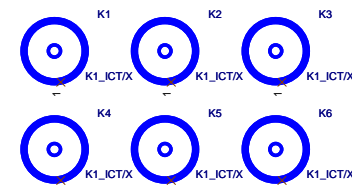
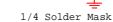
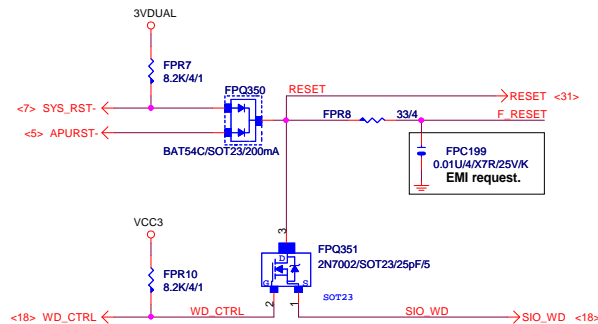
POWER SEQUENCE		
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Size	Custom	1.0
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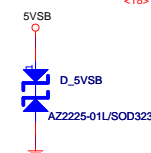




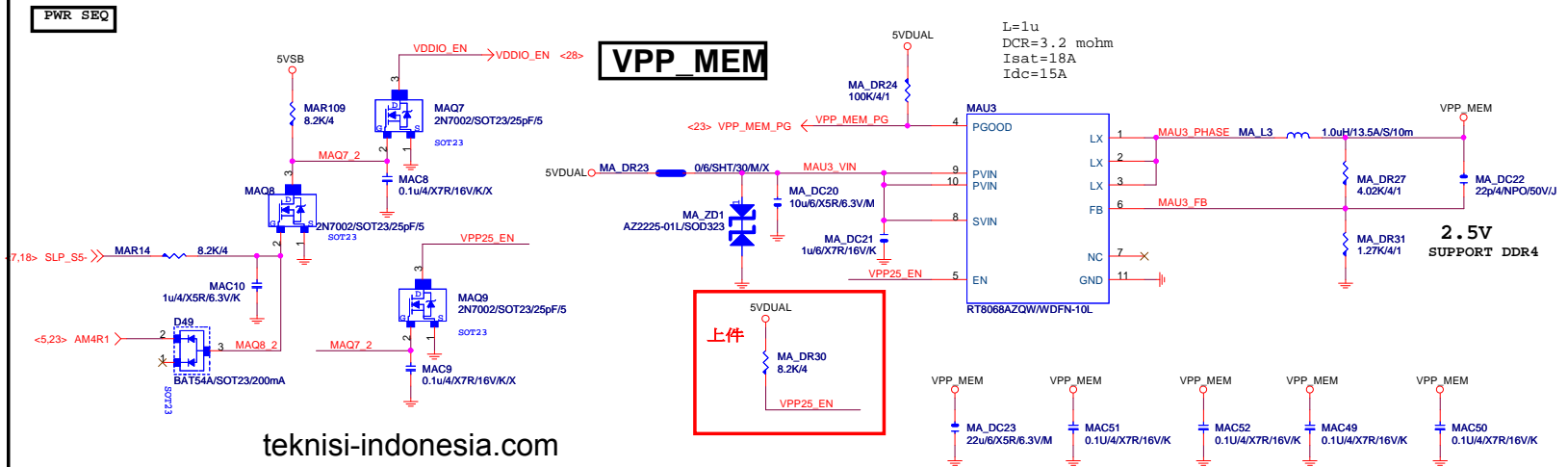
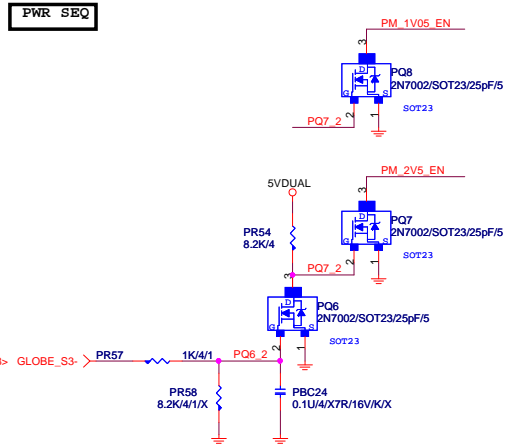
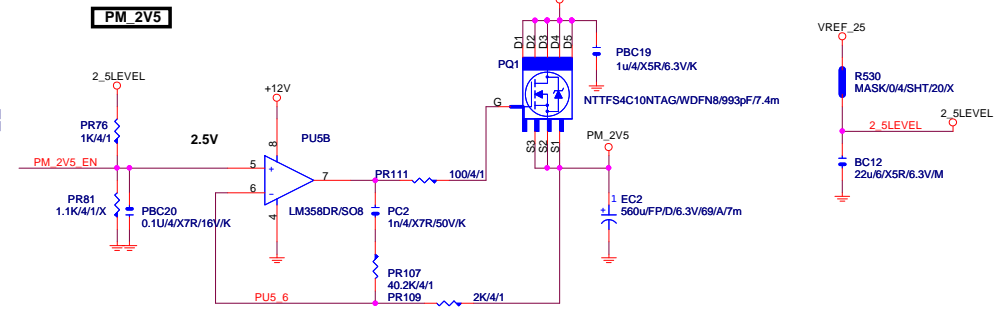
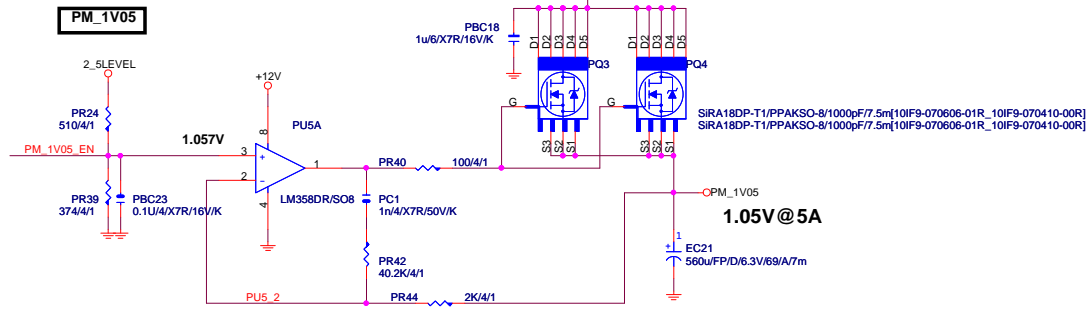




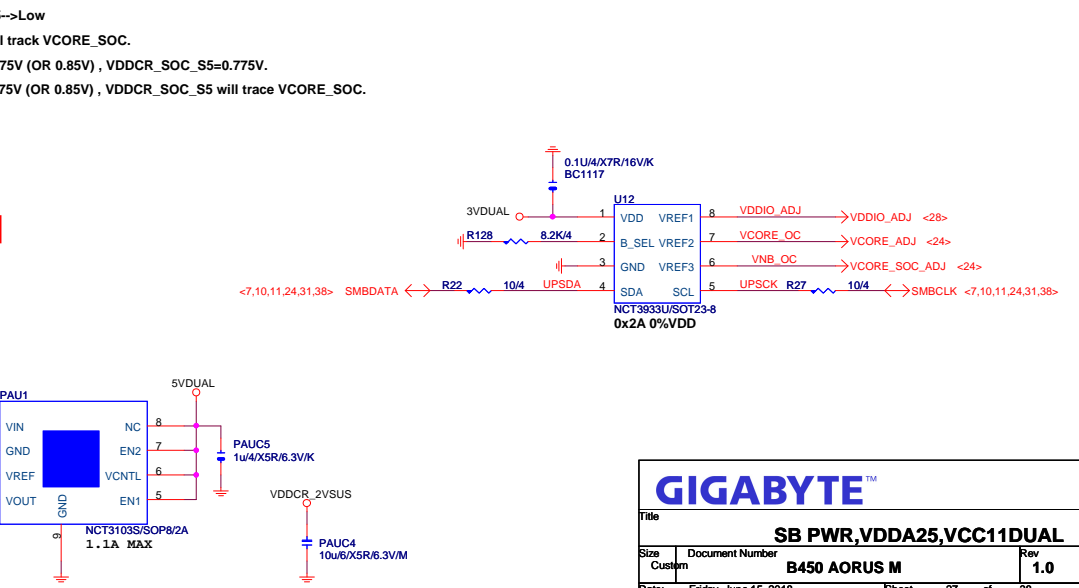
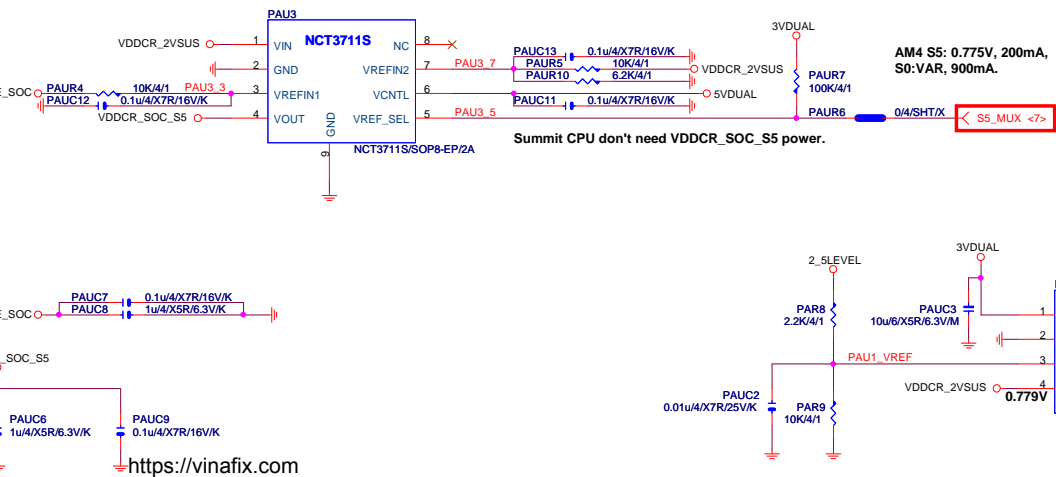
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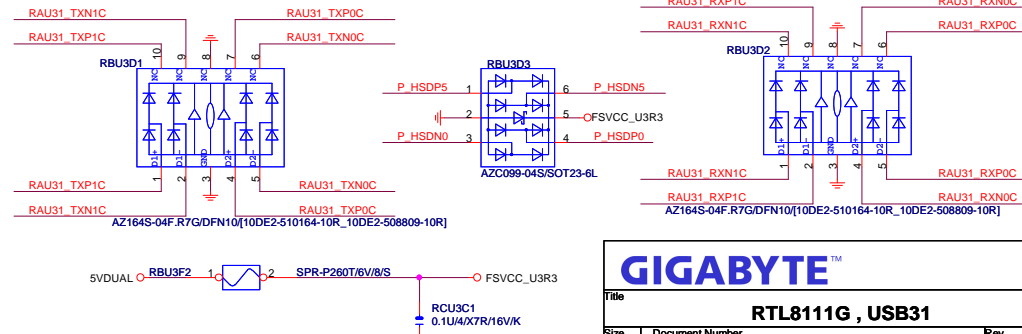
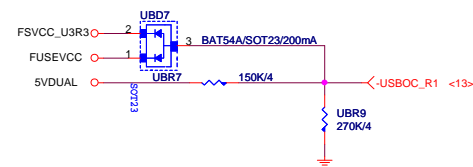
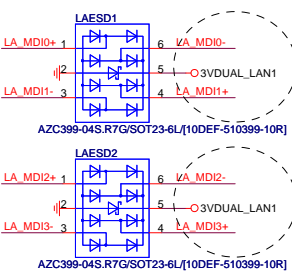
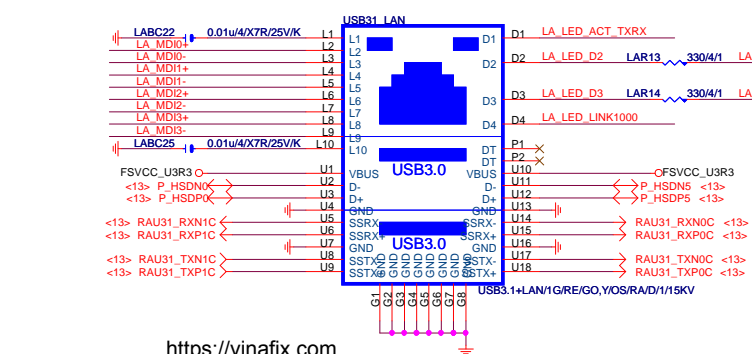
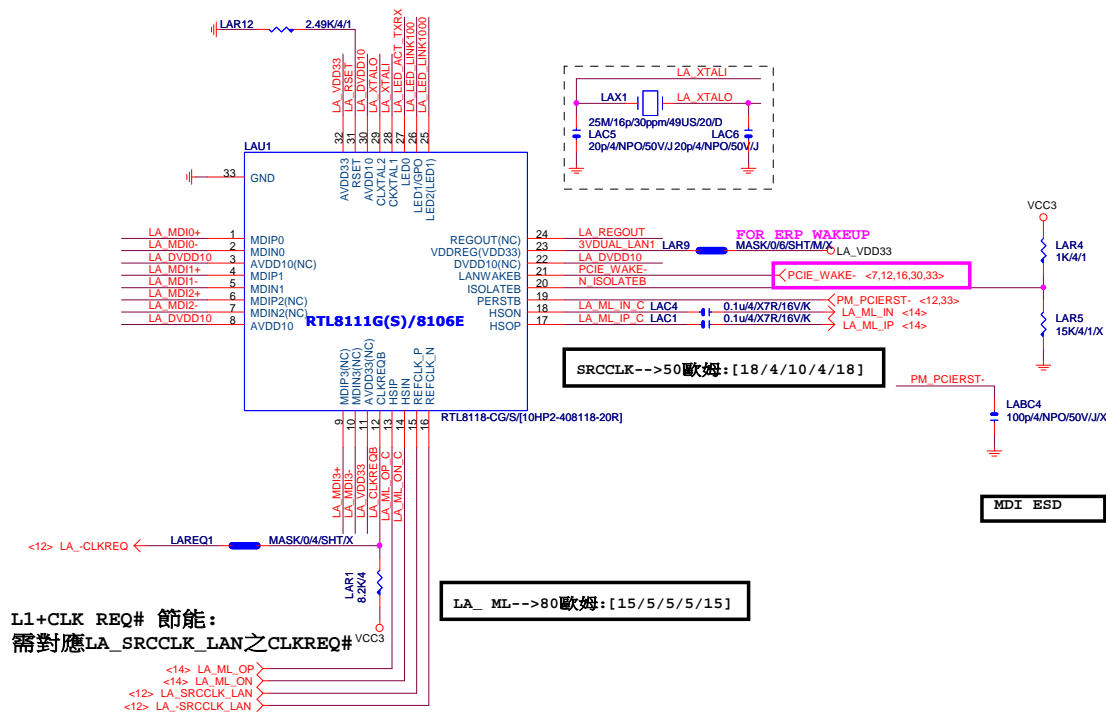
Title			
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Size	Document Number	Rev	
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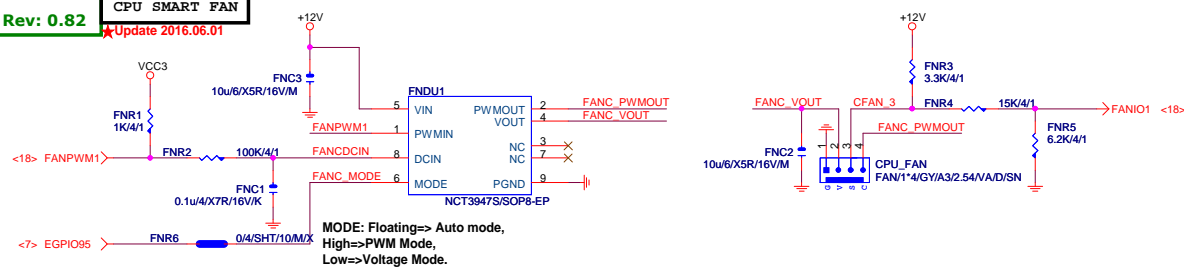


## VDDCR SOC S5

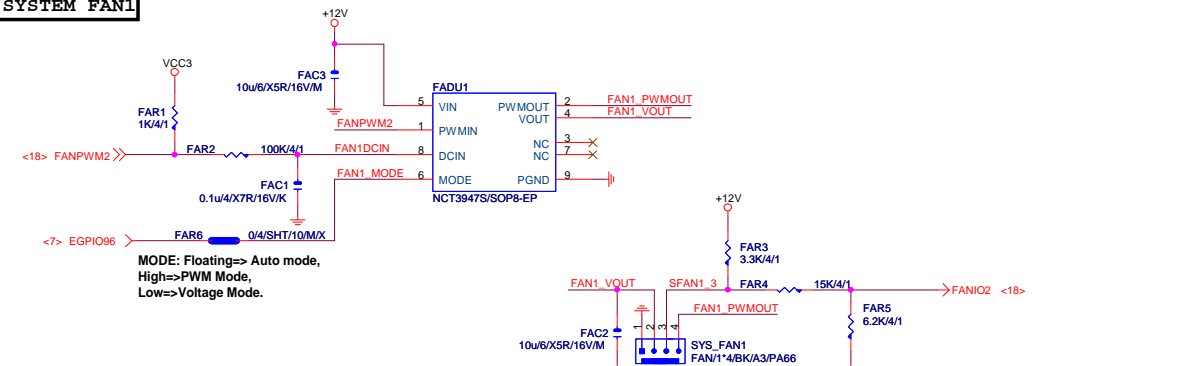




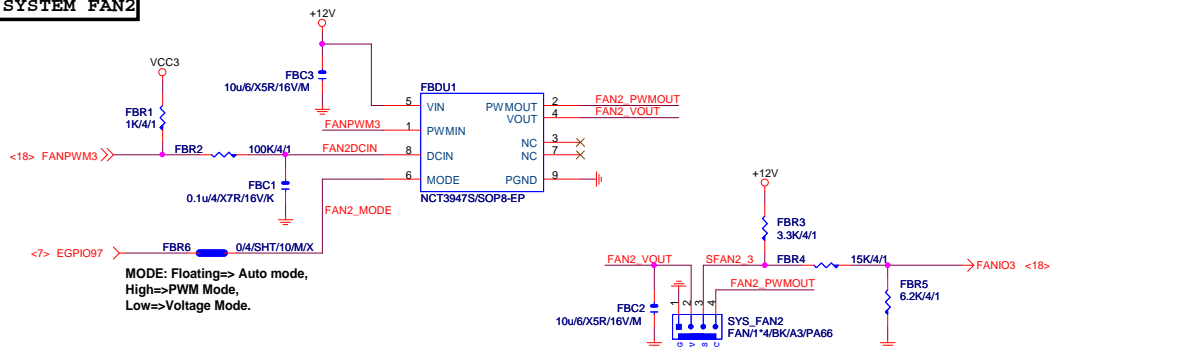




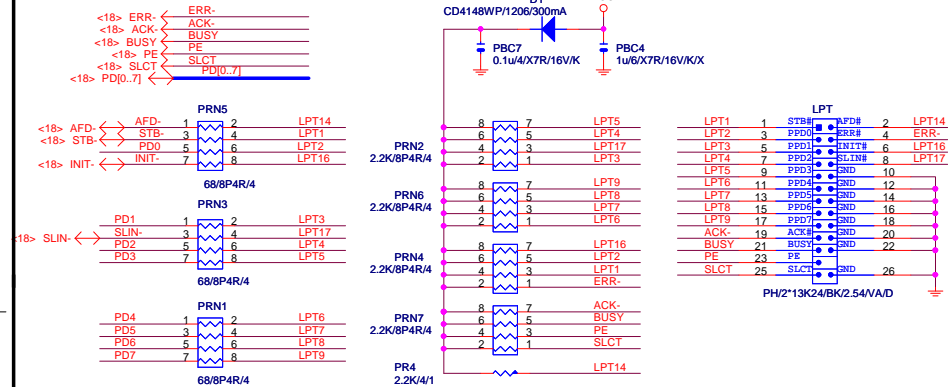
## SYSTEM FAN1



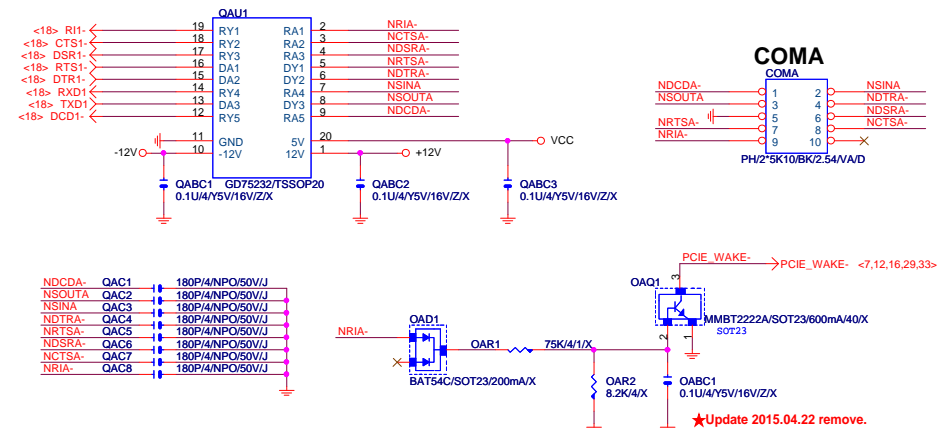
SYSTEM FAN2
-------------

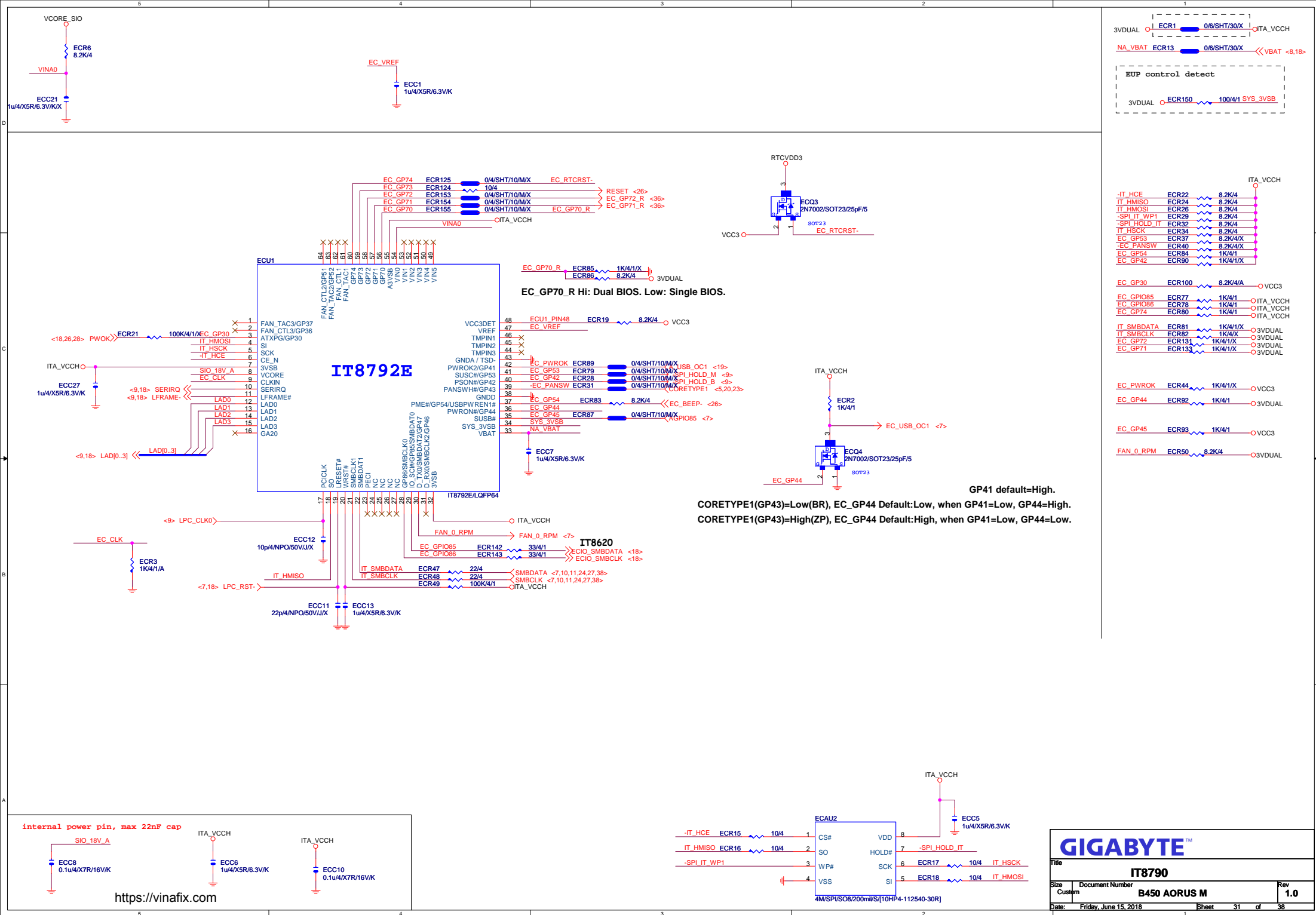


## LPT PORT



**COM PORT**





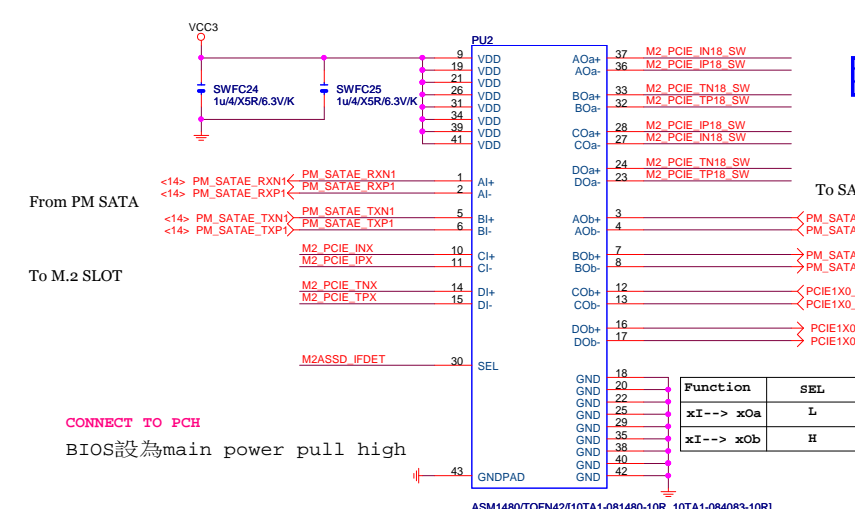
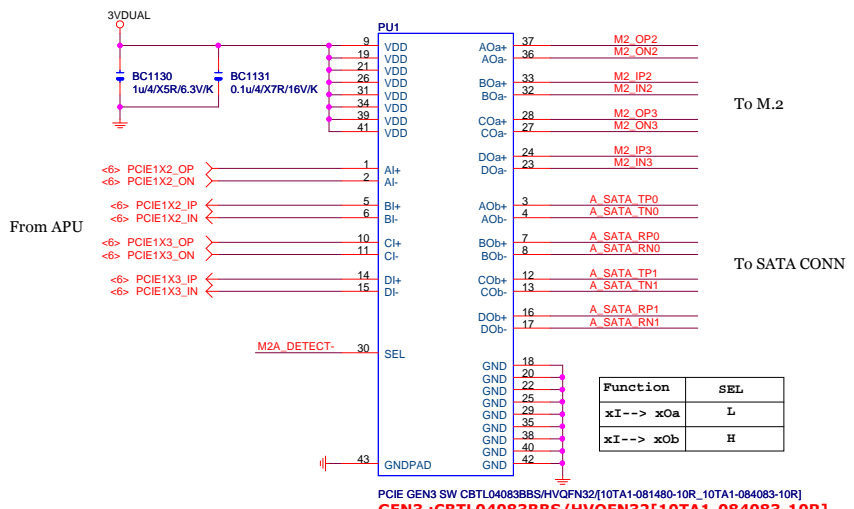
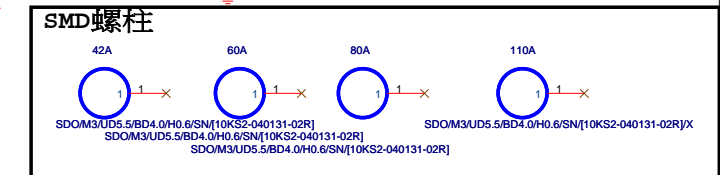
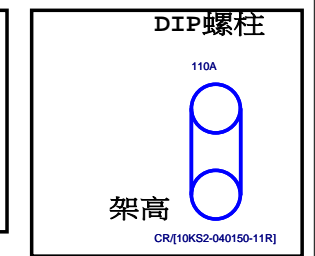
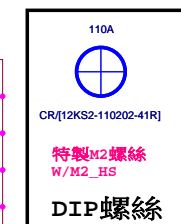
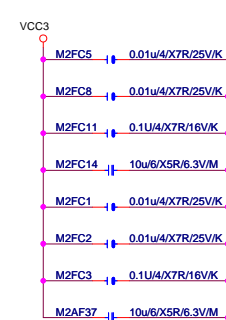
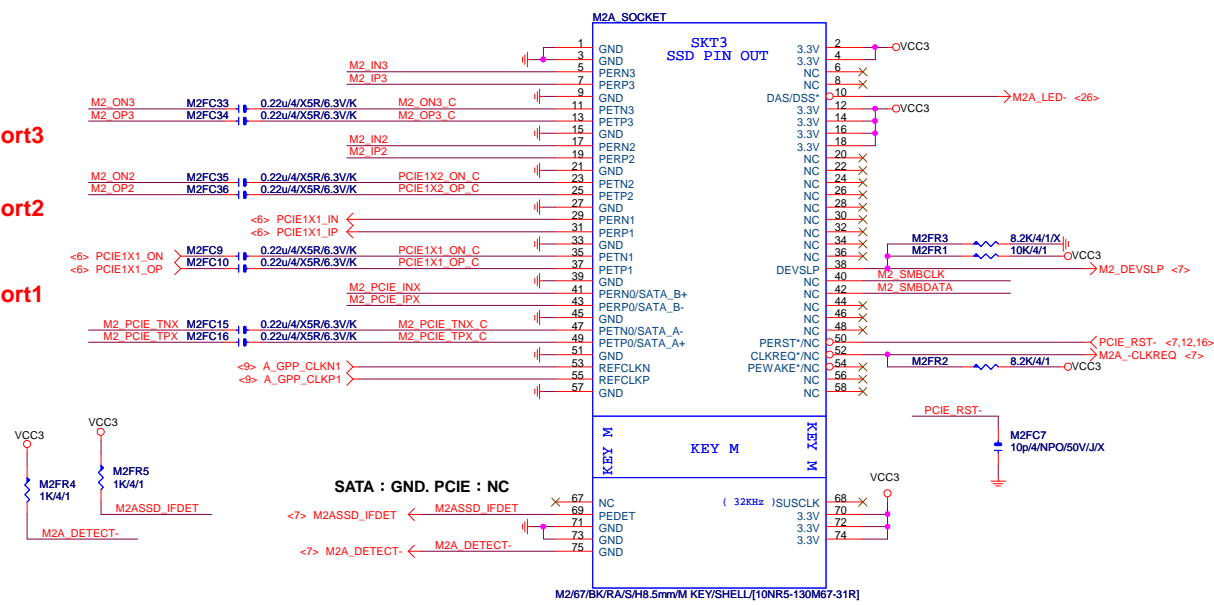
Rev 0.5

### M.2 Lane4 from AM4 port3

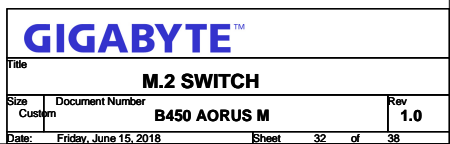
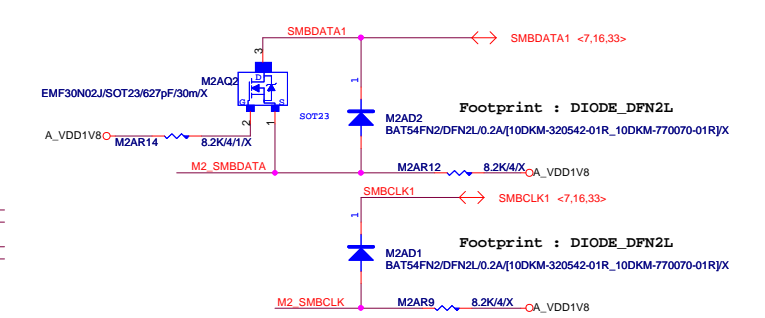
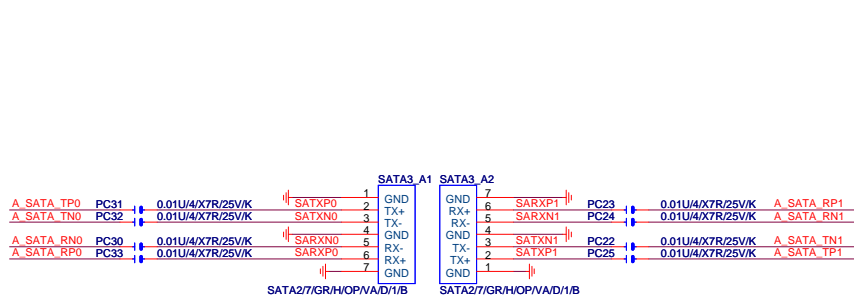
## M.2 Lane4 from AM4 port2

## M.2 Lane4 from AM4 port1

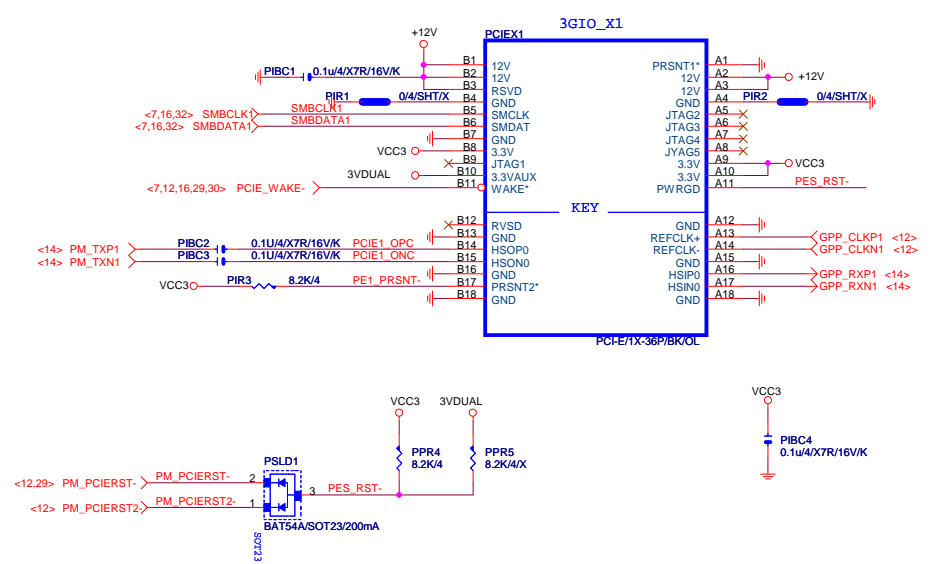
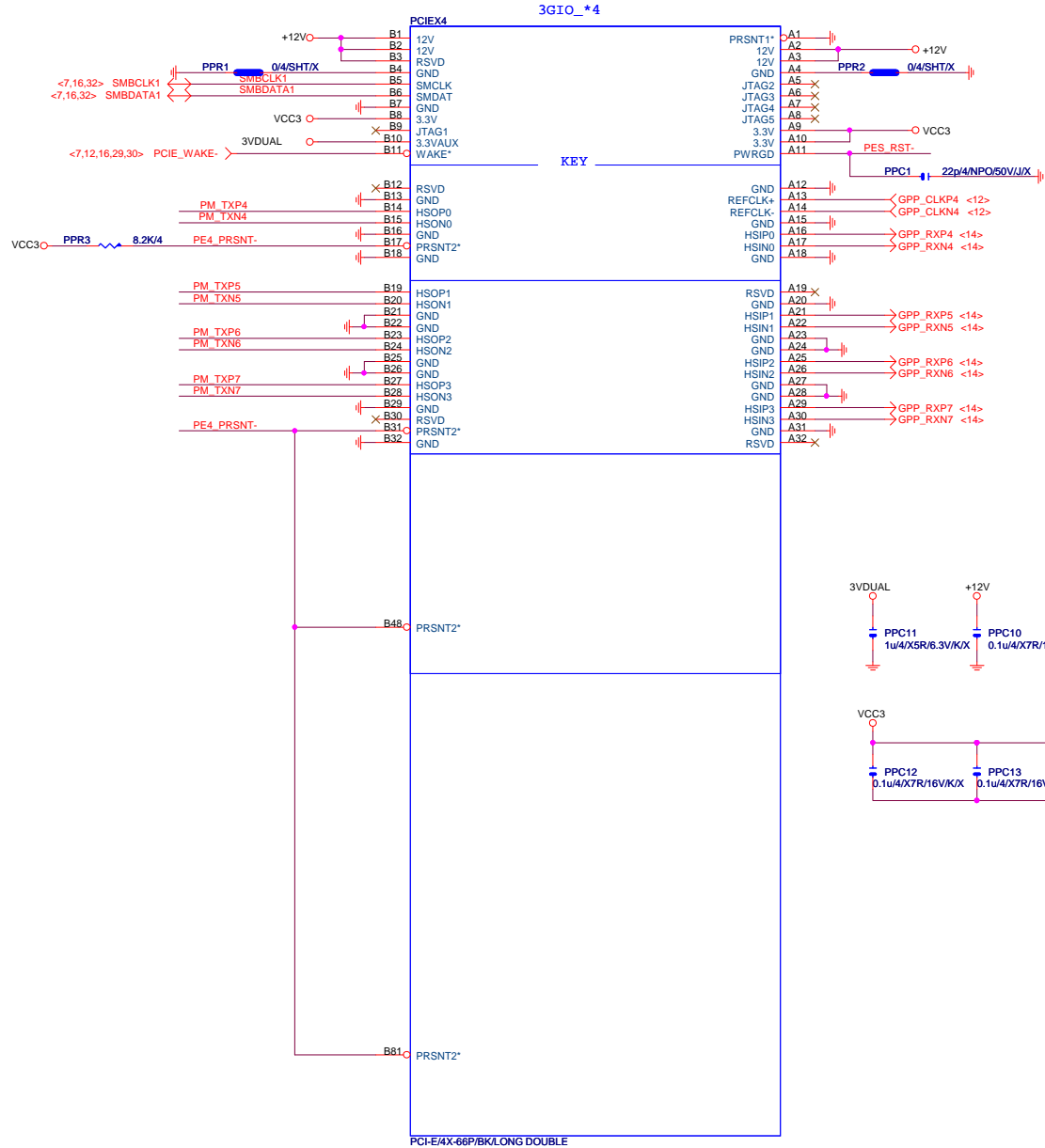
### by SWITCH Select



CONNECT TO PCH  
BIOS設為main power pull high



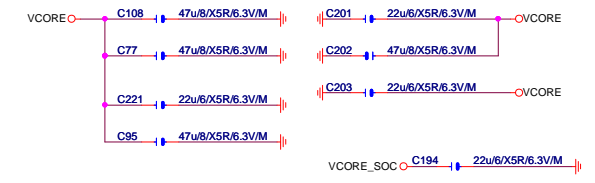
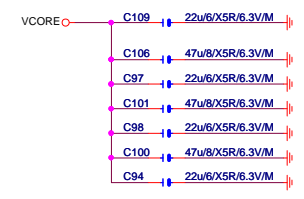
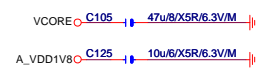
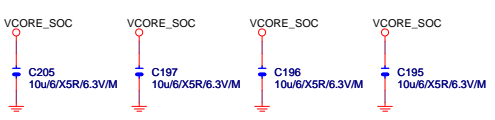
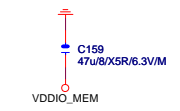
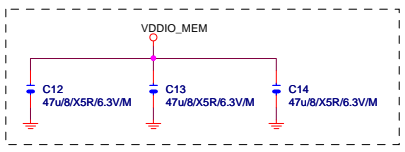
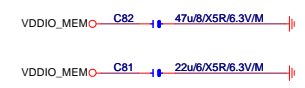
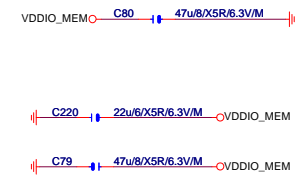
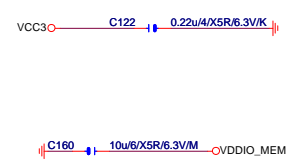
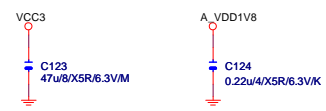
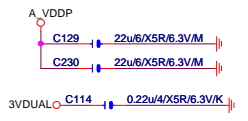
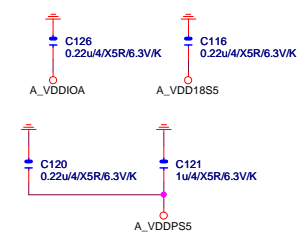
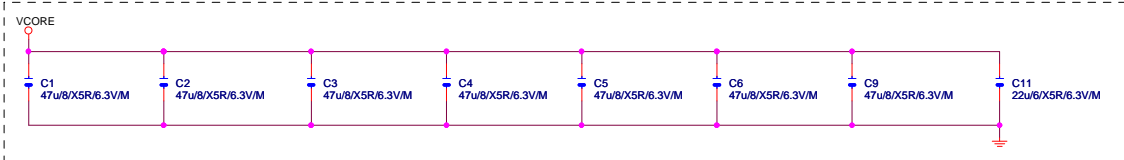




<14> GPP_TXP4	GPP_TXP4	PPC2	0.1u/4/X7R/16V/K	PM_TXP4
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<14> GPP_TXP5	GPP_TXP5	PPC4	0.1u/4/X7R/16V/K	PM_TXP5
<14> GPP_TXN5	GPP_TXN5	PPC5	0.1u/4/X7R/16V/K	PM_TXN5
<14> GPP_TXP6	GPP_TXP6	PPC6	0.1u/4/X7R/16V/K	PM_TXP6
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<b>GIGABYTE™</b>			
Title <b>PCIEx4 , PCIEx1</b>			
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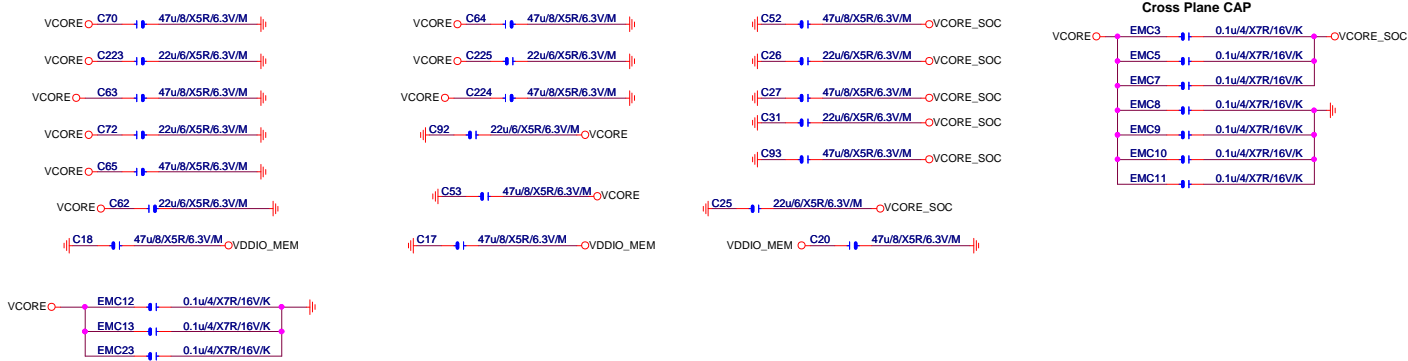


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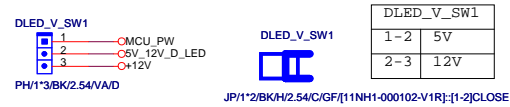
GIGABYTE™			
Title CPU BOTTOM			
Size Custom	Document Number B450 AORUS M		Rev 1.0
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CPU TOP CAVITY

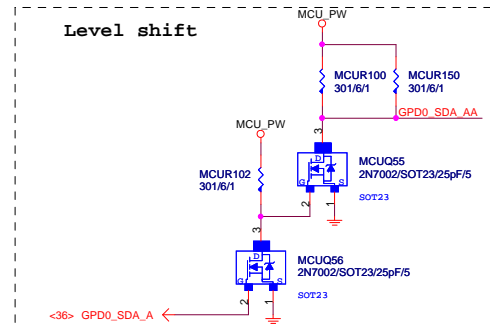
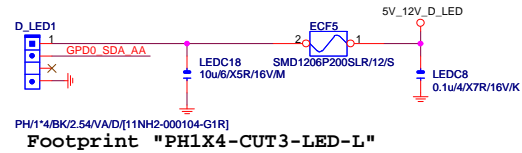




### 第六區 LED (靠近左上板邊位置)



## Digital LED Strip1

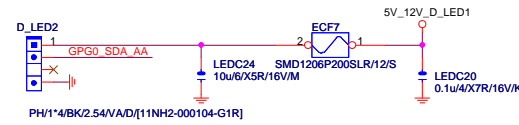


<https://vinafix.com>

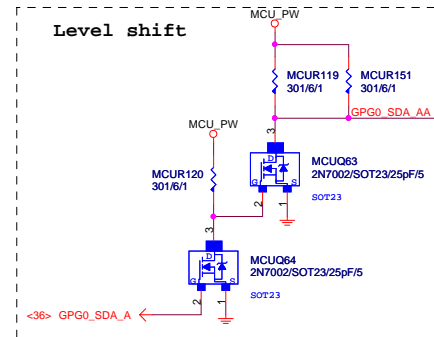
### 第七區 LED（靠近右下DDR板邊位置）



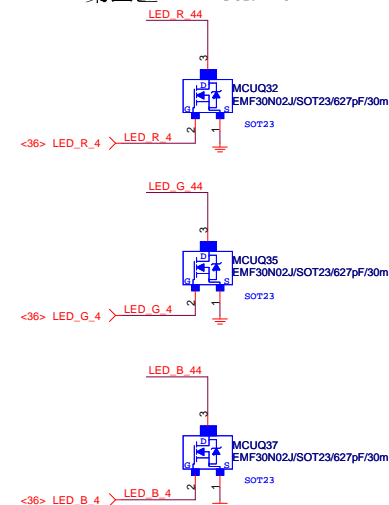
## Digital LED Strip2



Footprint "PH1X4-CUT3-LED-L"  
(for pin-name 與 model-name 同方向)

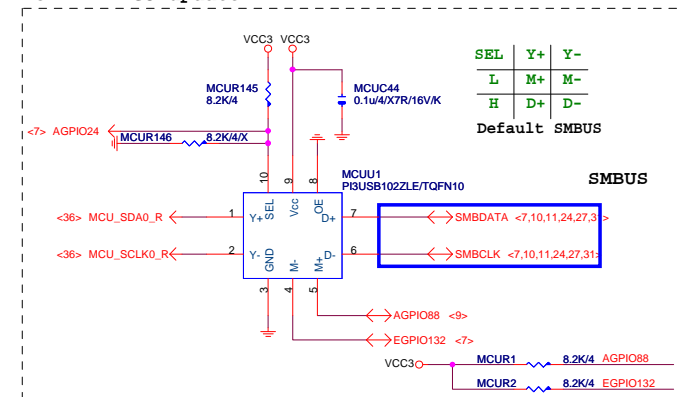


#### 第四區 LED CONTROL



FOR PCIEX8 側發光 LED\*4  
(位置在PCIEX8 SLOT兩側各4顆)

For AMD MCU update



1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
2. 背板 RGB LED 方向整板請統一如下  
(整板正極可統一朝下或朝上)
3. 正板 RGB LED 統一方向即可
4. MCU\_PW & MCU\_PW33電源一律走20mils
5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
6. MCU LED 出pin的走線4mils,如:LED\_R\_1,LED\_G\_1,LED\_B\_1 .....
7. LED RGBW rule :W/S=10/5 mils 如:LED\_R\_11,LED\_G\_11,LED\_B\_11,LED\_W.....  
(包含從晶體到排阻到LED的net)
8. Digital LED NET rule W/S=4/8 mils  
GPD0\_SDA\_B,GPD0\_SDA\_BB,GPD0\_SDA\_C,GPD0\_SDA\_CC